ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC100 Series Product Brief

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1 GENERAL DESCRIPTION

The NUC100 series are 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications need high-speed serial interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent traditional 8-bit microcontroller.

The NUC100 series embeds Cortex™-M0 core running up to 50MHz with 32K/64K/128K-byte embedded flash and 4K/8K/16K-byte embedded SRAM. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI/SSP, I^2C, I^2S, PWM Timer, GPIO, 12-bit ADC, Analog Comparator, Low Voltage Detector and Brown-out detector.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints.
- Wide operating voltage ranges from 2.5V to 5.5V
- Flash EPROM Memory
  - 32K/64K/128K bytes Flash EPROM for program code.
  - 4kB flash for ISP loader
  - Support In-system program(ISP) and In-application program(IAP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128kB system, fixed 4kB data flash for the 32kB and 64kB system.
  - Support 2-wire ICP update from ICE interface
  - Support fast parallel programming mode by external programmer.
- SRAM Memory
  - 4K/8K/16k bytes embedded SRAM.
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals.
- Clock Control
  - Flexible selection for different applications.
  - Build-in 22MHz OSC (Trimmed to 1%) for system operation, and low power 10KHz OSC for watchdog and wakeup sleep operation.
  - Support one PLL, up to 50MHz, for high performance system operation.
  - External 12MHz crystal input for precise timing operation.
  - External 32 kHz crystal input for RTC function and low power system operation.

- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable.
  - I/O pin can be configured as interrupt source with edge/level setting.
  - High driver and high sink IO mode support.
- Timers
  - 4 sets of 24-bit timer with 8-bit pre-scaler.
  - Counter auto reload.
- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Switchable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support time tick interrupt
  - Support wake up function.
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs.
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - Up to eight 16-bit digital Capture timers(shared with PWM timers) provide eight rising/falling capture inputs.
  - Support Capture interrupt
- UART
  - Up to three compatible 16550 UART devices.
  - UART ports with flow control (TX, RX, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Support IrDA(SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode

- SPI
  - Up to four sets of SPI device.
  - Master up to 16 Mbps / Slave up to 10 Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Byte Sleeping mode in 32-bit transmission
  - Support PDMA mode
- I^2C
  - Two sets of I^2C device.
  - Master/Slave up to 1Mbit/s (Fast-mode Plus)
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clocks allow versatile rate control.
  - I2C-bus controllers support multiple address recognition (two slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- ADC
  - 12-bit SAR ADC with 800ksps
  - Up to 8-ch single-end mode or 4-ch differential mode
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by S/W, external pins
  - Support PDMA mode
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up

- One built-in temperature sensor with 1℃ resolution.
- Brown-out detector
  - With 4 levels: 4.5V/3.8V/2.7V/2.2V
  - Support Brownout Interrupt and Reset option
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
    - LQFP 100-pin / 64-pin / 48-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Products Selection Guide

3.1.1 NUC100 series Advance Line Selection Guide (Medium density)

Part number	Flash	SRAM	Connectivity			I²S	PWM	Comp.	ADC	Timer	RTC	ISP ICP	I/O	Package
			UART	SPI	I²C									
NUC100LE3AN	128 KB	16 KB	2	1	2	1	6	1	8x12-bit	4x32-bit	v	v	up to 35	LQFP48
NUC100LD3AN	64 KB	16 KB	2	1	2	1	6	1	8x12-bit	4x32-bit	v	v	up to 35	LQFP48
NUC100RE3AN	128 KB	16 KB	3	2	2	1	6	2	8x12-bit	4x32-bit	v	v	up to 49	LQFP64
NUC100RD3AN	64 KB	16 KB	3	2	2	1	6	2	8x12-bit	4x32-bit	v	v	up to 49	LQFP64
NUC100VE3AN	128 KB	16 KB	3	4	2	1	8	2	8x12-bit	4x32-bit	v	v	up to 80	LQFP100
NUC100VD3AN	64 KB	16 KB	3	4	2	1	8	2	8x12-bit	4x32-bit	v	v	up to 80	LQFP100
NUC100VD2AN	64 KB	8 KB	3	4	2	1	8	2	8x12-bit	4x32-bit	v	v	up to 80	LQFP100

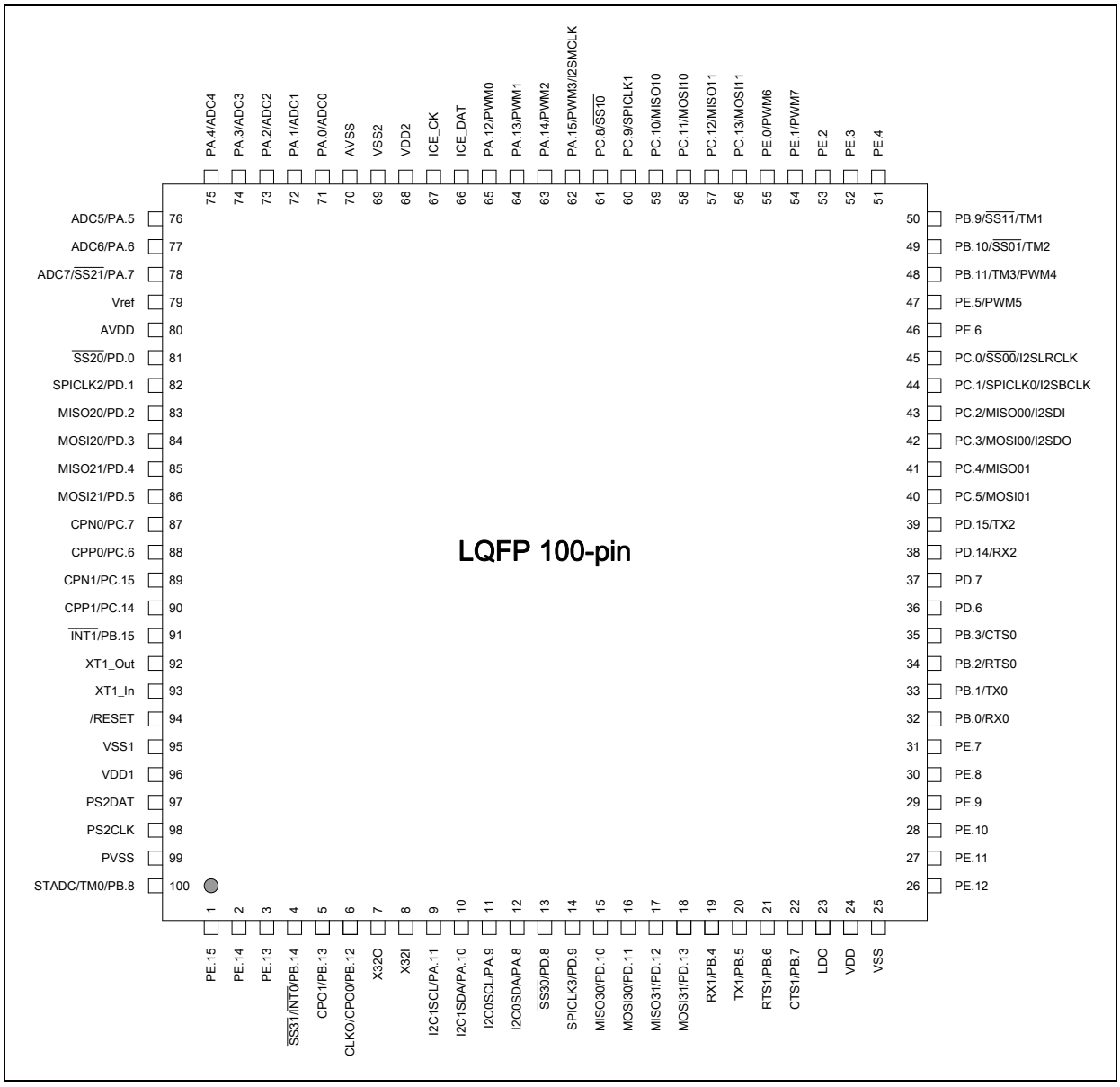
3.1.2 NUC100 series Advance Line Selection Guide (Low density)

※ The following parts support one-channel PDMA

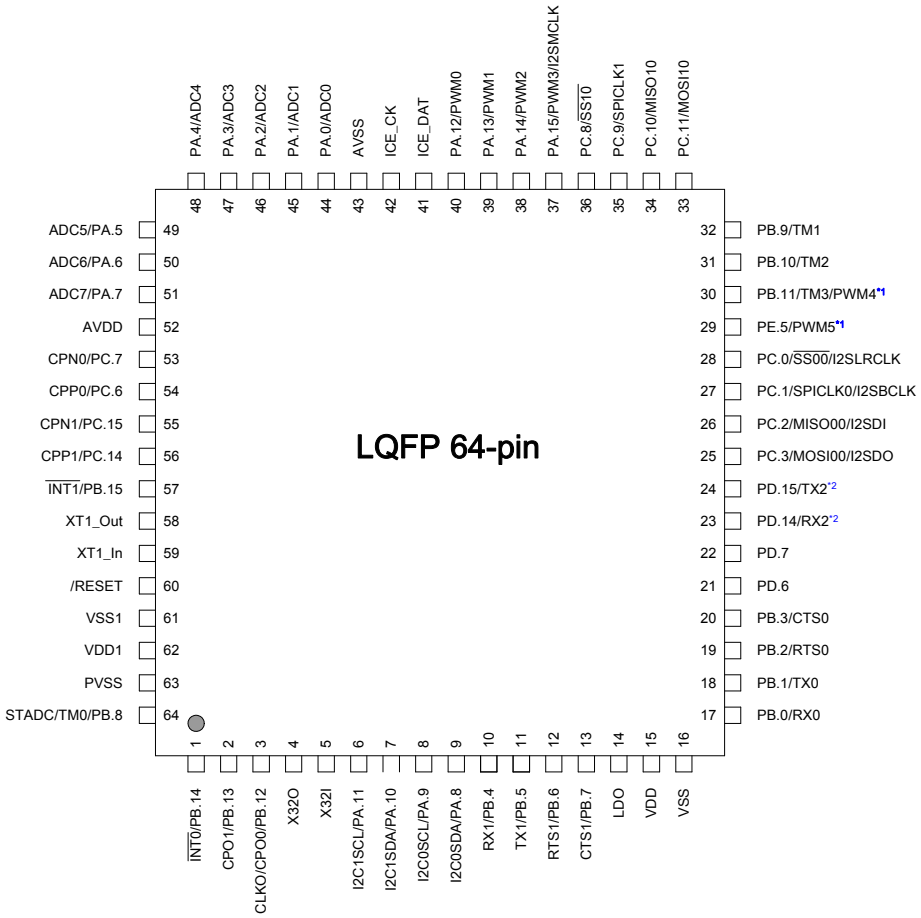
Part number	Flash	SRAM	Connectivity			I²S	PWM	Comp.	ADC	Timer	RTC	ISP ICP	I/O	Package
			UART	SPI	I²C									
NUC100LD2AN	64 KB	8 KB	2	1	2	1	4	1	8x12-bit	4x32-bit	v	v	up to 35	LQFP48
NUC100LD1AN	64 KB	4 KB	2	1	2	1	4	1	8X12-Bit	4x32-bit	v	v	up to 35	LQFP48
NUC100LC1AN	32 KB	4 KB	2	1	2	1	4	1	8X12-Bit	4x32-bit	v	v	up to 35	LQFP48
NUC100RD2AN	64 KB	8 KB	2	2	2	1	4	2	8x12-bit	4x32-bit	v	v	up to 49	LQFP64
NUC100RD1AN	64 KB	4 KB	2	2	2	1	4	2	8X12-Bit	4x32-bit	v	v	up to 49	LQFP64
NUC100RC1AN	32 KB	4 KB	2	2	2	1	4	2	8X12-Bit	4x32-bit	v	v	up to 49	LQFP64

3.2 Pin Configuration

3.2.1 NUC100 LQFP 100 pin

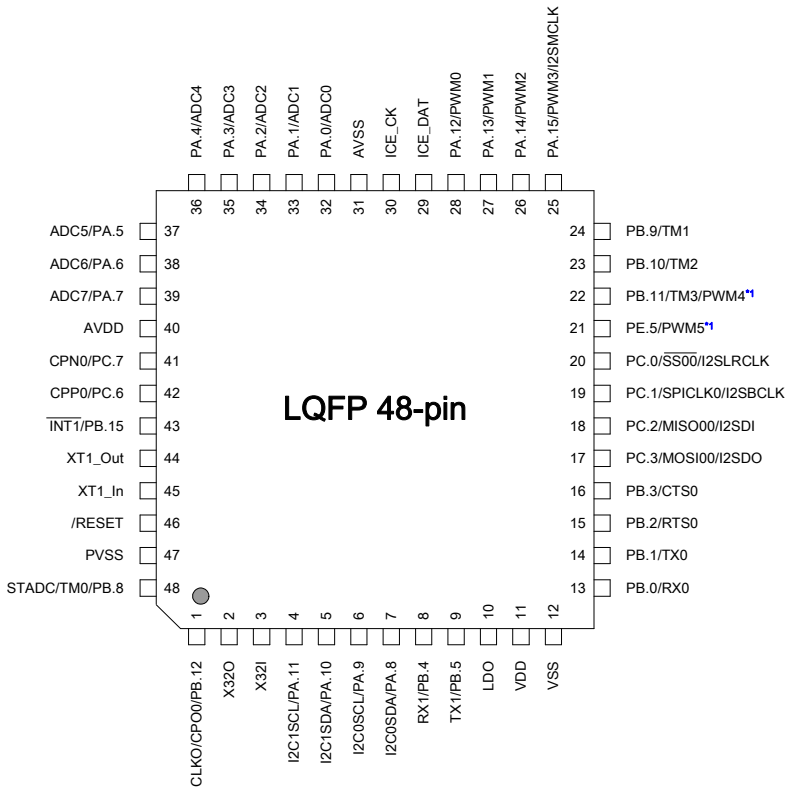


3.2.2 NUC100 LQFP 64 pin



Note:
1. PWM4 and PWM5 are only supported in medium density version.
2. TX2 and RX2 are only supported in medium density version.

3.2.3 NUC100 LQFP 48 pin



Note:
1. PWM4 and PWM5 are only supported in medium density version.

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

4.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage (bypass = 0)	V_{LDO}	-10%	2.45	+10%	V	V_{DD} > 2.7V
LDO Output Voltage (bypass = 0)	V_{LDO}	-10%	V_{DD}	+10%	V	V_{DD} < 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50Mhz	I_{DD1}		54		mA	V_{DD}= 5.5V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		31		mA	V_{DD}=5.5V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		51		mA	V_{DD} = 3V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		28		mA	V_{DD} = 3V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12Mhz	I_{DD5}		22		mA	V_{DD} = 5.5V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		14		mA	V_{DD} = 5.5V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		20		mA	V_{DD} = 3V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD8}		12		mA	V_{DD} = 3V@12Mhz, disable all IP and disable PLL, XTAL=12MHz

Operating Current Normal Run Mode @ 4Mhz	I_{DD9}		15		mA	V_{DD} = 5V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		11		mA	V_{DD} = V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		13		mA	V_{DD} = 3V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		9		mA	V_{DD} = 3V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50Mhz	I_{IDLE1}		38		mA	V_{DD}= 5.5V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		35		mA	V_{DD} = 3V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12Mhz	I_{IDLE5}		13		mA	V_{DD} = 5.5V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5.5		mA	V_{DD} = 5.5V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		12		mA	V_{DD} = 3V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE8}		4		mA	V_{DD} = 3V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Idle Mode @ 4Mhz	I_{IDLE9}		8.5		mA	V_{DD} = 5V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE10}		3.5		mA	V_{DD} = V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		7		mA	V_{DD} = 3V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		2.5		mA	V_{DD} = 3V@4Mhz, disable all IP and disable PLL, XTAL=4MHz

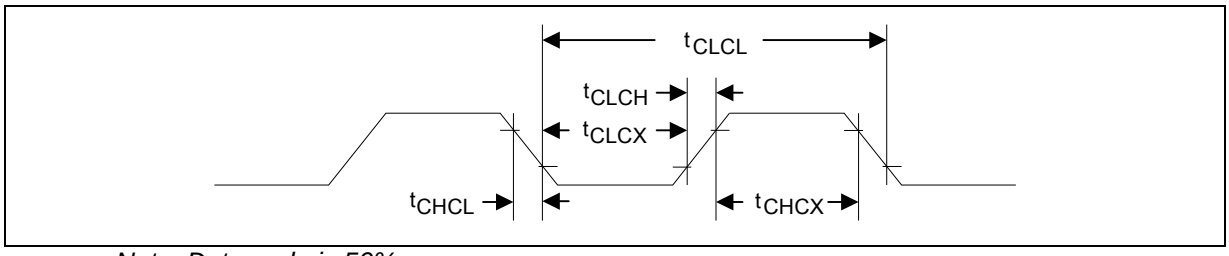
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		23		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		18		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		28		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		22		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET [1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidiretional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	1.0	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.2	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.8		
		0	-	0.4		
Input High Voltage X32O[*2]	V_{IH4}	3.5	-	V_{DD} +0.2		
		2.4	-	V_{DD} +0.2		
Negative going threshold (Schmitt input), /RST	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input), /RST	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Internal /RST pin pull up resistor	R_{RST}	50		100	KΩ	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	

Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V .

4.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	-	nS	
Clock Low Time	t_{CLCX}	20	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

4.3.1 External XTAL1 Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V

4.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

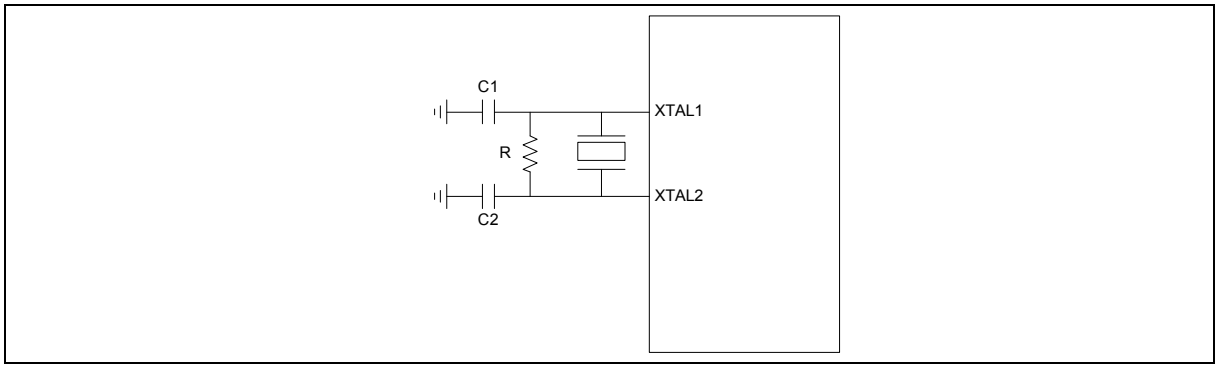


Figure 4-1 Typical Crystal Application Circuit

4.3.2 External 32kHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	-	5.5	V
Operating current	V_{DD} = 5V	-	5	-	uA

4.3.3 Internal 22.1184MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-1	-	+1	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-3	-	+3	%
Operating current	V_{DD} =5V	-	500	-	uA

4.3.4 Internal 10kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes form LDO.

4.4 Analog Characteristics

4.4.1 Specification of 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±3	-	LSB
Integral nonlinearity error	INL	-	±4	-	LSB
Offset error	EO	-	±1	10	LSB
Gain error (Transfer gain)	EG	-	1	1.005	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	20	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	800	Ksps
Supply voltage	V_{LDO}	-	2.5	-	V
	VADD	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	IDDA	-	1.5	-	mA
Reference voltage	VREF	-	VDDA	-	V
Reference current (Avg.)	IREFP	-	1	-	mA
Input voltage range	VIN	0	-	VREF	V
Capacitance	CIN	-	5	-	pF

4.4.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage (bypass=0)	-10%	2.45	+10%	V	LDO output voltage
Output Voltage (bypass=1)	-10%	Input Voltage	+10%	V	Input Voltage < 2.7V
Temperature	-40	25	85	oC	
Quiescent Current (PD=0, bypass=0)	-	100	-	uA	
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Quiescent Current (PD=1, bypass=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

4.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

4.4.4 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

4.4.5 Specification of Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

4.4.6 Specification of Temperature Sensor

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply voltage[1]	2.5	-	5.5	V	
Temperature	-40	-	125	℃	
Current consumption	6.4	-	10.5	uA	
Gain	-1.95	-2	-2.05	mV/℃	
Offset	688	708	730	mV	Temp=0 ℃

Notes:

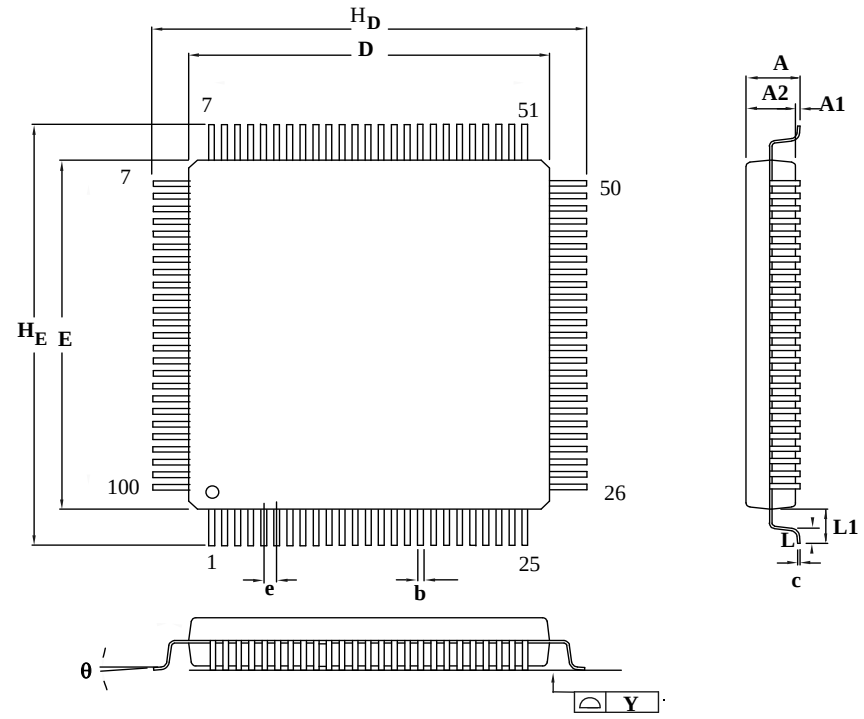
1. Internal operation voltage comes form LDO.

4.4.7 Specification of Comparator

PARAMETER	MIN.	TYP.	MAX.	CONDITION
Temperature	-40℃	25 ℃	85℃	-
VDD	2.4	3	5.5	-
VDD current	-	20uA	40uA	20uA@VDD=3V
Input offset voltage	-	5mV	15mV	-
Output swing	0.1	-	VDD-0.1	-
Input common mode range	0.1	-	VDD-1.2	-
DC gain	-	70dB	-	-
Propagation delay	-	200ns	-	@VCM=1.2V & VDIFF=0.1V
Comparison voltage	10mV	20mV	-	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis
Hysteresis	-	±10mV	-	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V
Wake up time	-	-	2us	@CINP=1.3V CINN=1.2V

5 PACKAGE DIMENSIONS

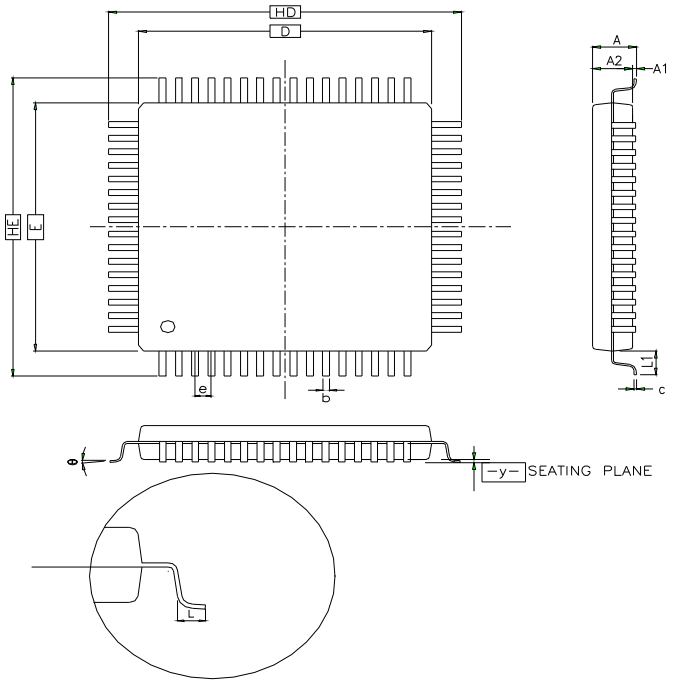
5.1.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

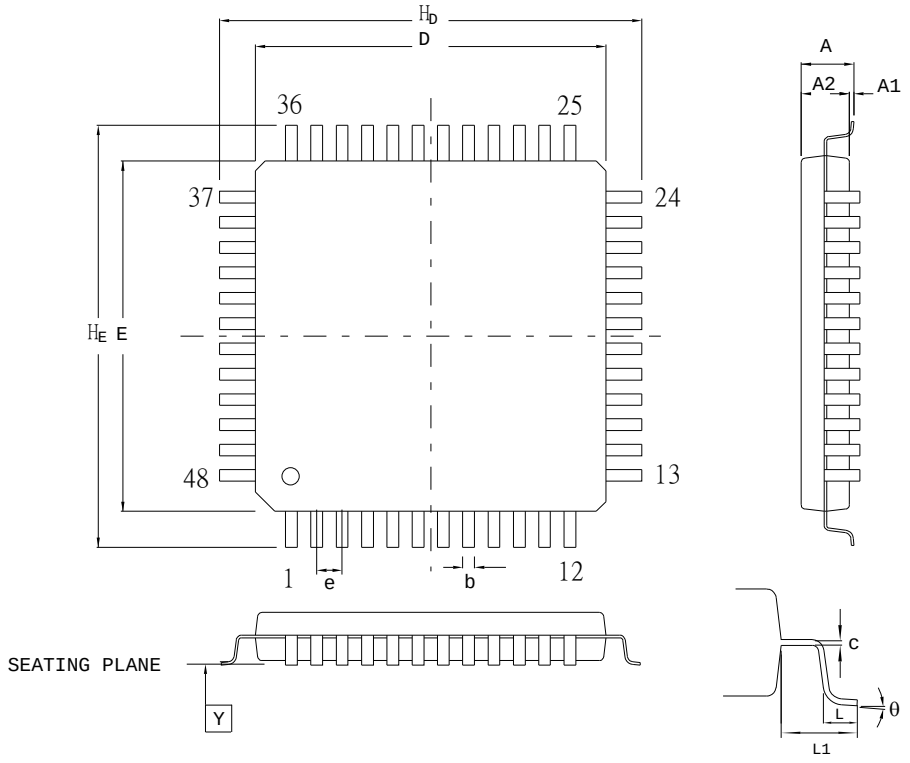
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

5.1.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

5.1.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

6 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.12	April 9, 2010	-	initial issued
V1.13	May 31, 2010	4.2	1. Add operation current of DC characteristics
V1.14	Aug. 23, 2010	5.2	1.Modify operation current of DC characteristics

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