

# **Spartan-6 FPGA Memory Interface Solutions**

## ***User Guide***

UG416 June 22, 2011



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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/2/09	1.0	Initial Xilinx release.
2/23/10	1.1	Updated <a href="#">Figure 1-30</a> . Revised the text below the <a href="#">Calibrated Input Termination</a> bullet on <a href="#">page 30</a> . Added Xilinx ISim to first paragraph in <a href="#">Functional Simulation</a> , <a href="#">page 47</a> .
3/3/10	1.2	Added note about device migration to <a href="#">page 31</a> .
10/5/10	1.3	Added ARM® AMBA® specifications web link to <a href="#">References</a> . Added paragraph about creating an MCB base memory interface in the EDK environment to the first page of <a href="#">Chapter 1, Getting Started</a> . Added note after <a href="#">step 1</a> and updated <a href="#">step 5</a> in <a href="#">Setting up a New Project</a> , <a href="#">page 13</a> . Added information to <a href="#">step 1</a> in <a href="#">Selecting a Memory Standard</a> . Updated <a href="#">Figure 1-10</a> and <a href="#">Figure 1-23</a> . Added description of axi_s6_ddrx instances after <a href="#">Figure 1-11</a> . Updated Frequency bullet in <a href="#">Setting Controller Options</a> , <a href="#">page 19</a> . Added information to <a href="#">step 8</a> , updated <a href="#">step 9</a> , and added <a href="#">step 10</a> and <a href="#">Figure 1-27</a> in <a href="#">Multi-Port Configuration</a> . Updated first paragraph, <a href="#">step 14</a> , and <a href="#">step 14</a> of <a href="#">Setting FPGA Options</a> , <a href="#">page 30</a> . Updated and added note after <a href="#">Figure 1-37</a> . Added <a href="#">Table 1-1</a> . Added <a href="#">&lt;component name&gt;/example_design/rtl/mcb_controller</a> , <a href="#">page 37</a> . Updated and added note after <a href="#">Table 1-6</a> . Updated parameter description of CMD_PATTERN in <a href="#">Table 1-11</a> . Added last paragraph (about changing command patterns) to <a href="#">Custom Command Sequences</a> . Added <a href="#">Chapter 2, EDK Flow Details</a> . Changed “ctrl_state[4:0]” to “ctrl_state[144:0]”, “ctrl_cmd” to “ctrl_cmd[2:0]”, and “cal_state[3:0]” to “cal_state[144:0]” in <a href="#">Table 3-1</a> . Added “ASCII radix” to descriptions of ctrl_state[144:0] and cal_state[144:0] in <a href="#">Table 3-1</a> .
10/18/10	1.3.1	Revised document file name.

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Date	Version	Revision
06/22/11	1.4	Chapter 1: Removed step 14 about calibration memory address and associated figure from <a href="#">Setting FPGA Options, page 30</a> . Revised notes on <a href="#">page 37</a> and <a href="#">page 38</a> . Revised <a href="#">Functional Simulation, page 47</a> . Chapter 2: Revised <a href="#">Interface Clock, page 58</a> . Added <a href="#">Simulation Considerations, page 61</a> . Updated ui_clk in <a href="#">Table 2-2</a> . Chapter 3: Added <a href="#">Figure 3-3</a> .



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# About This Guide

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This document describes the design tool flow and debug procedures for external memory interfaces implemented with the memory controller block (MCB) in Spartan®-6 FPGAs. For more information on the functionality and operation of the MCB, refer to *Spartan-6 FPGA Memory Controller User Guide* [Ref 1].

## Guide Contents

This manual contains these chapters:

- [Chapter 1, Getting Started](#), describes how to use the MIG tool available in the CORE Generator™ tool or Embedded Development Kit (EDK) environment to implement a memory interface based on the MCB.
- [Chapter 2, EDK Flow Details](#), provides additional details on generating an MCB design when invoking the MIG tool from the Xilinx® Platform Studio (XPS) in the EDK environment.
- [Chapter 3, Debugging MCB Designs](#), defines a step-by-step debugging procedure to assist in the identification and resolution of any issues that might arise during each phase of the design process.

## References

These references provide additional information useful with this document:

1. [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*
2. [UG683](#), *EDK Concepts, Tools, and Techniques*
3. [UG111](#), *Embedded System Tools Reference Guide*
4. [UG626](#), *Synthesis and Simulation Design Guide*
5. ChipScope™ Pro Logic Analyzer tool  
<http://www.xilinx.com/tools/cspro.htm>
6. [UG628](#), *Command Line Tools User Guide*, COMPXLIB
7. PlanAhead™ Design Analysis tool  
<http://www.xilinx.com/tools/planahead.htm>
8. [UG612](#), *Xilinx Timing Constraints User Guide*
9. [UG199](#), *Virtex®-5 FPGA ML561 Memory Interfaces Development Board User Guide*
10. ARM® AMBA® Specifications  
<http://www.arm.com/products/system-ip/amba/amba-open-specifications.php>

## Additional Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

<http://www.xilinx.com/support>.

For a glossary of technical terms used in Xilinx documentation, see:

[http://www.xilinx.com/support/documentation/sw\\_manuals/glossary.pdf](http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf).

## List of Acronyms

The following acronyms are used in this document:

Acronym	Definition
AXI	Advanced Extensible Interface
BSB	Base System Builder
DDR	Double Data Rate
EDK	Embedded Development Kit
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
IBIS	I/O Buffer Information Specification
ICON	Integrated Controller
ILA	Integrated Logic Analyzer
LFSR	Linear Feedback Shift Register
LPDDR	Low Power Double Data Rate
LUT	Look-Up Table
MC	Memory Controller
MCB	Memory Controller Block
MIG	Memory Interface Generator
ODT	On-Die Termination
PRBS	Pseudo Random Binary Sequence
RAM	Random Access Memory
RLDRAM	Reduced-Latency Dynamic Random Access Memory
RTL	Register Transfer Level
SDRAM	Synchronous Dynamic Random Access Memory
UCF	User Constraints File
VIO	Virtual I/O
XPS	Xilinx Platform Studio