Spartan-6 FPGA Memory Interface Solutions

User Guide

UG416 June 22, 2011

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/2/09	1.0	Initial Xilinx release.
2/23/10	1.1	Updated Figure 1-30. Revised the text below the Calibrated Input Termination bullet on page 30. Added Xilinx ISim to first paragraph in Functional Simulation, page 47.
3/3/10	1.2	Added note about device migration to page 31.
10/5/10	1.3	Added ARM® AMBA® specifications web link to References. Added paragraph about creating an MCB base memory interface in the EDK environment to the first page of Chapter 1, Getting Started. Added note after step 1 and updated step 5 in Setting up a New Project, page 13. Added information to step 1 in Selecting a Memory Standard. Updated Figure 1-10 and Figure 1-23. Added description of axi_s6_ddrx instances after Figure 1-11. Updated Frequency bullet in Setting Controller Options, page 19. Added information to step 8, updated step 9, and added step 10 and Figure 1-27 in Multi-Port Configuration. Updated first paragraph, step 14, and step 14 of Setting FPGA Options, page 30. Updated and added note after Figure 1-37. Added Table 1-1. Added <component name>/example_design/rtl/mcb_controller, page 37. Updated and added note after Table 1-6. Updated parameter description of CMD_PATTERN in Table 1-11. Added last paragraph (about changing command patterns) to Custom Command Sequences. Added Chapter 2, EDK Flow Details. Changed “ctrl_state[4:0]“ to “ctrl_state[144:0]”, “ctrl_cmd” to “ctrl_cmd[2:0]”, and “cal_state[3:0]” to ”cal_state[144:0]” in Table 3-1. Added “ASCII radix”to descriptions of ctrl_state[144:0] and cal_state[144:0] in Table 3-1.
10/18/10	1.3.1	Revised document file name.

Date	Version	Revision
06/22/11	1.4	Chapter 1: Removed step 14 about calibration memory address and associated figure from Setting FPGA Options, page 30. Revised notes on page 37 and page 38. Revised Functional Simulation, page 47. Chapter 2: Revised Interface Clock, page 58. Added Simulation Considerations, page 61. Updated ui_clk in Table 2-2. Chapter 3: Added Figure 3-3.

Table of Contents

Chapter 2: EDK Flow Details

Chapter 3: Debugging MCB Designs

About This Guide

This document describes the design tool flow and debug procedures for external memory interfaces implemented with the memory controller block (MCB) in Spartan®-6 FPGAs. For more information on the functionality and operation of the MCB, refer to *Spartan-6 FPGA Memory Controller User Guide* [Ref 1].

Guide Contents

This manual contains these chapters:

- Chapter 1, Getting Started, describes how to use the MIG tool available in the CORE Generator™ tool or Embedded Development Kit (EDK) environment to implement a memory interface based on the MCB.
- Chapter 2, EDK Flow Details, provides additional details on generating an MCB design when invoking the MIG tool from the Xilinx® Platform Studio (XPS) in the EDK environment.
- Chapter 3, Debugging MCB Designs, defines a step-by-step debugging procedure to assist in the identification and resolution of any issues that might arise during each phase of the design process.

References

These references provide additional information useful with this document:

1. UG388, *Spartan-6 FPGA Memory Controller User Guide*
2. UG683, *EDK Concepts, Tools, and Techniques*
3. UG111, *Embedded System Tools Reference Guide*
4. UG626, *Synthesis and Simulation Design Guide*
5. ChipScope™ Pro Logic Analyzer tool
   http://www.xilinx.com/tools/cspro.htm
6. UG628, *Command Line Tools User Guide*, COMPXLIB
7. PlanAhead™ Design Analysis tool
   http://www.xilinx.com/tools/planahead.htm
8. UG612, *Xilinx Timing Constraints User Guide*
9. UG199, *Virtex®-5 FPGA ML561 Memory Interfaces Development Board User Guide*
10. ARM® AMBA® Specifications
    http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

Additional Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

http://www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf.

List of Acronyms

The following acronyms are used in this document:

Acronym	Definition
AXI	Advanced Extensible Interface
BSB	Base System Builder
DDR	Double Data Rate
EDK	Embedded Development Kit
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
IBIS	I/O Buffer Information Specification
ICON	Integrated Controller
ILA	Integrated Logic Analyzer
LFSR	Linear Feedback Shift Register
LPDDR	Low Power Double Data Rate
LUT	Look-Up Table
MC	Memory Controller
MCB	Memory Controller Block
MIG	Memory Interface Generator
ODT	On-Die Termination
PRBS	Pseudo Random Binary Sequence
RAM	Random Access Memory
RLDRAM	Reduced-Latency Dynamic Random Access Memory
RTL	Register Transfer Level
SDRAM	Synchronous Dynamic Random Access Memory
UCF	User Constraints File
VIO	Virtual I/O
XPS	Xilinx Platform Studio