Fujitsu Microelectronics Europe
Application Note

FMEMCU-AN-900098-14

F²MC-16LX FAMILY

16-BIT MICROCONTROLLER

ALL 16LX SERIES

HARDWARE SET UP

APPLICATION NOTE

Revision History

Date	Issue
2003-08-18	V1.0; First version; MWi
2004-01-16	V1.1; Specification changed; MWi
2004-03-09	V1.2; Pin connection chapter added; MWi
2004-03-22	V1.3; Corrections done
2004-04-30	V1.4; Chapter 3 upgraded; MWi

This document contains 18 pages.

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Contents

0 Introduction

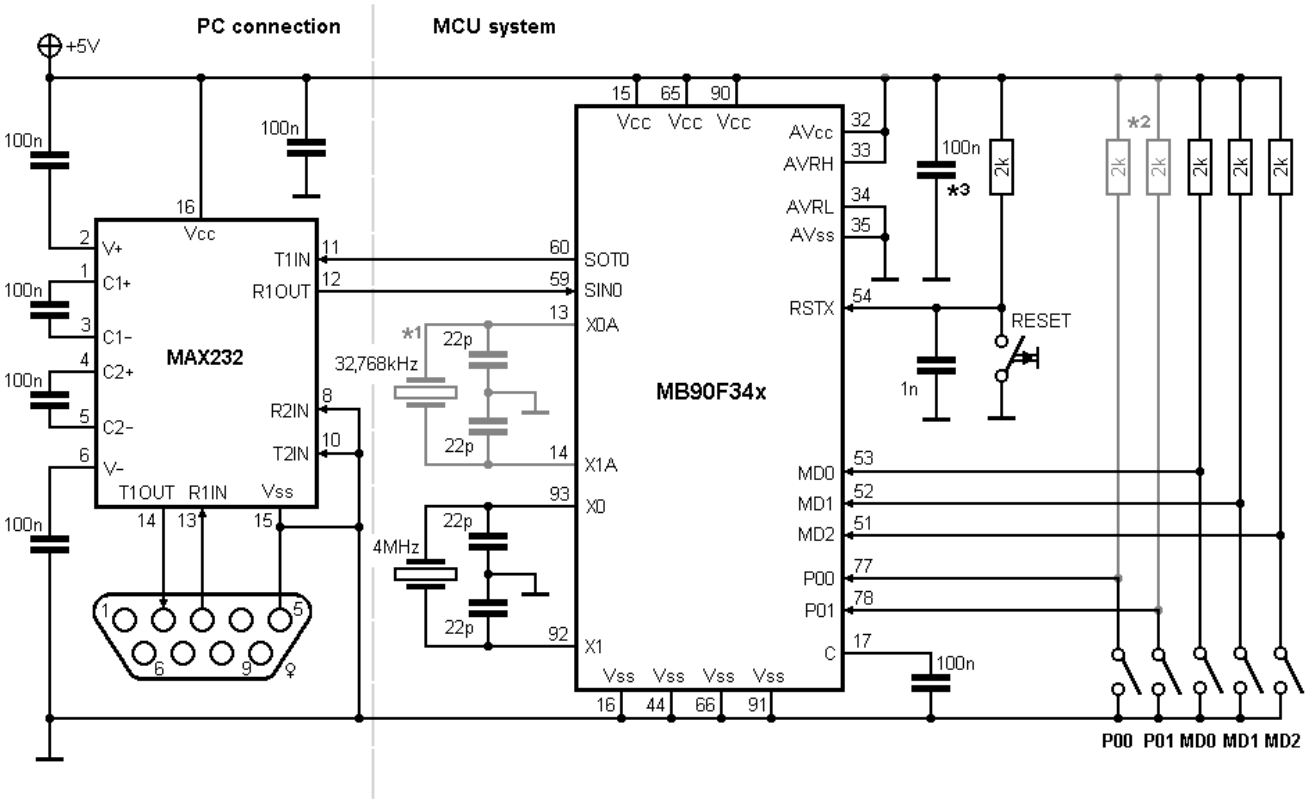
This application note describes how to set up a hardware environment for Fujitsu 16LX MCUs. As an example the MB90F34x MCU is used.

1 Minimal System

THIS CHAPTER GIVES AN EXAMPLE OF A MINIMUM HARDWARE SYSTEM

1.1 Schematic

The following graphic shows a schematic of a minimum hardware system. Note that for other MCU families a different pinning is needed.



*1 only needed for dual clock devices.
*2 only needed if other than asynchronous programming is used
*3 please refer to chapter 2

1.2 Serial Interface

The “PC connection” section is only needed, if no 5V external serial data lines for programming are existing. The MAX232 is a standard level shifter, which converts the 5V levels of the MCU to ±12V RS232V24 levels and vice versa.

If you use a 3.3V MCU a MAX3232 is recommend.

1.3 Power supply

The power supply should be 5 Volts ±10% for normal usage. If a different supply voltage is used please refer to the MB90340 data sheet.

1.4 Analog Digital Converter Supply Pins

The analog converter supply pins (AVcc, AVss, AVRH, AVRL) should be connected even if the ADC of the MCU is not used. Please refer to our application note *an-900084-ADC* for using the ADC and pin connection.

1.5 Analog Input Pins

Because the ADC works with an internal sample capacitor the input impedance and external capacity must be low. Fujitsu recommends an input impedance of not more than 15k Ohm. Choose the external capacity as low as possible (about 1 nF for EMI protection).

1.6 Reset Pin (RSTX)

The reset pin should be pulled up to Vcc with a 2-5k resistor. To reset the MCU a switch connects this pin to Vss (Ground). Additionally a capacitor has to be connected between Vss and the reset pin for debouncing the switch and for EMI protection. From experience Fujitsu recommend a capacity of not more than 1 nF. This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with a RSTX-Switch and low EMI protection.

If the device has a HSTX pin, this pin should be connected to RSTX.

Exception:

Using MB90F548*GHDS* please refer to the data sheet and hardware manual for HSTX and RTSX pin connection and behavior.

For further information please refer to the general application note *an-reset-16lx-900074*.

1.7 C Pin

A 100nF capacitor *must* be connected to the C pin of the MCU. Otherwise the MCU may not operate correct or will be damaged in worst case. Also see chapter 2.

1.8 Clock Source

A clock source must be provided to the MCU. Therefore crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

Note, that for non-S-devices (Families: MB90[F]54x, MB90[F]57x, MB90[F]58x) the 32768Hz sub clock *must* be connected.

Please also refer to the chapter *Outline/Precautions for Device Handling* in the corresponding hardware manual for details.

1.9 Mode Pins

The mode pins signalize the MCU the current operation mode. For a minimal system only two modes are necessary: Flash-Asynchronous-Serial-Programming-Mode and Free-Running-Mode. They should be pulled-up with 2k resistors.

If other programming modes are used, which needs a high level on the port pins (P00, P01), these pins has to pulled-up with a 2k resistor, if using a switch. (Be aware that the port pins then have a different electrical character if used as outputs.)

For these programming modes and methods please refer to the application notes *an-900031-flash-prog* and *an-900095-flash_prog2*.

The following settings are used for the both modes mentioned above:

1.9.1 Flash-Asynchronous-Serial-Programming-Mode

P00	P01	MD0	MD1	MD2
closed	closed	closed	open	open

1.9.2 Free-Running-Mode

P00	P01	MD0	MD1	MD2
open	open	open	open	closed

1.10 NC Pins

Please read Chapter 3 for how to proceed with unused (not connected) pins.

2 Layout and Electromagnetic Compatibility

THIS CHAPTER GIVES SOME TIPS FOR LAYOUT DESIGN

2.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design has to be observed.

The most critical point is the C pin because this is the connection to the internal 3.3V supply for the MCU core. Thus a decoupling capacitor has to be placed very near to this pin.

Also the ground and Vcc routing has to be done carefully. Vcc lines should be routed in star shape. We recommend a Vss ground plane *on the mounting side* just under the MCU. For both Vcc and Vss only *one* connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. Decoupling capacitors (DeCaps) has to be placed as nearest as possible to the related pins. If they are placed too far away their function becomes useless.

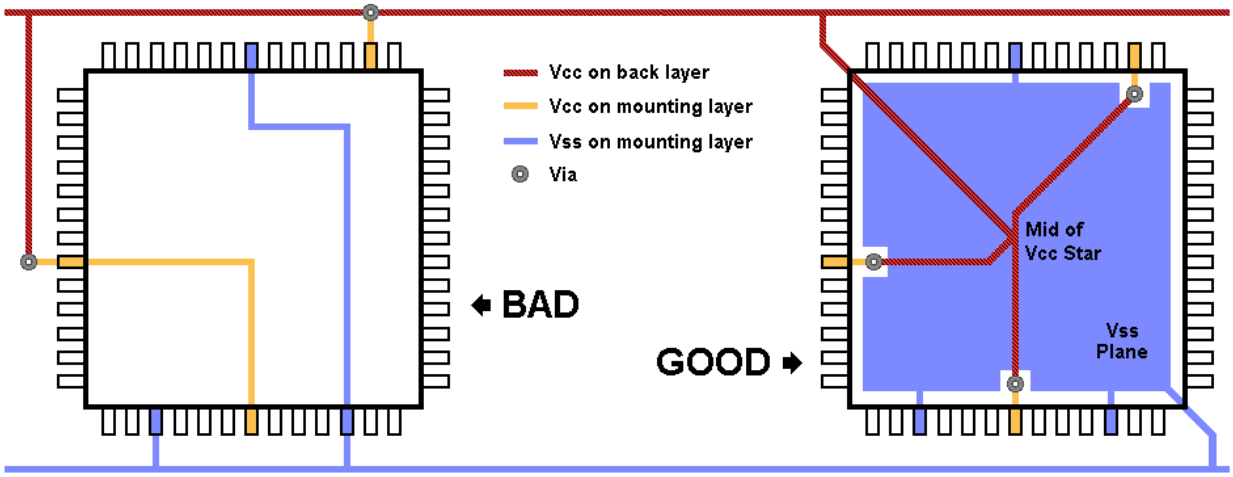
If crystals are used, they have to be placed as nearest as possible to the Xn(A) pins.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU.

2.2 Power Line Routing

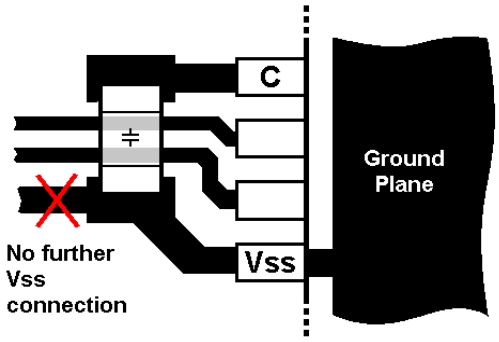
In general the Vcc and Vss lines should not be routed in “chains”, but in “star shape”. For Vss a ground plane is recommended which covers the chip package, and is connected in *one* point to Vss of the whole circuit.

Below is a example of a bad and a good power line routing:

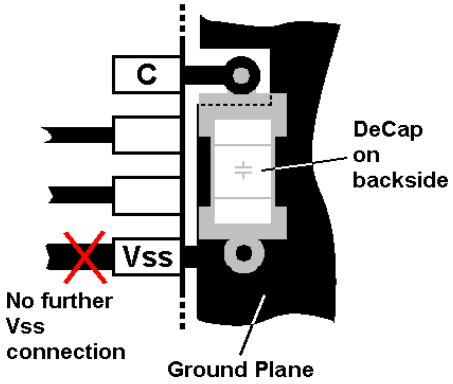


2.3 C Pin Decoupling

The following routing and placement for single sided metal layer is recommended (Note, that in all following illustrations the mounting metal layer is drawn in black and the back side metal layer in gray):

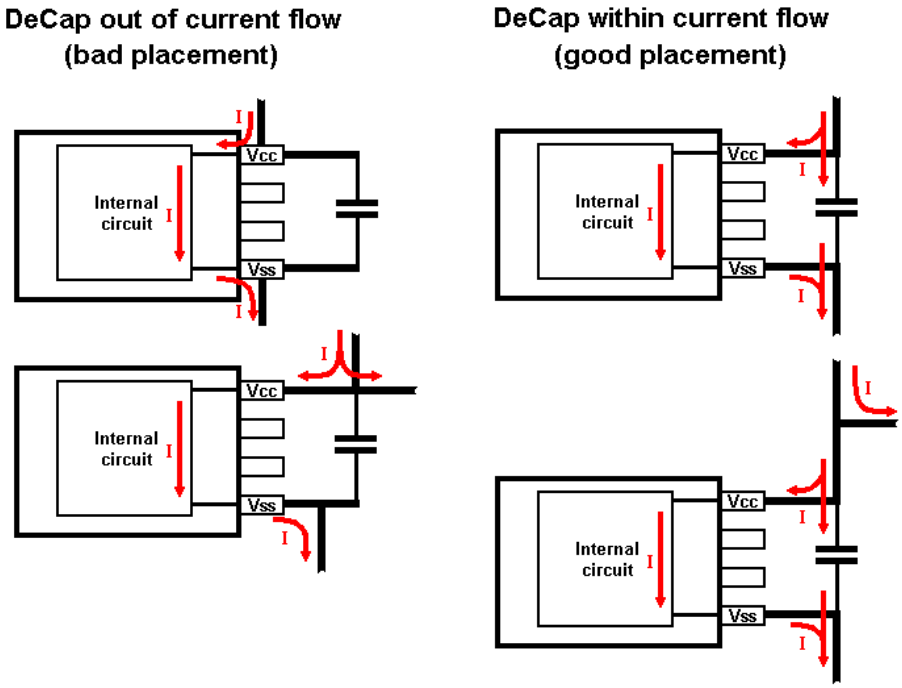


The following routing and placement for double sided metal layer is recommended. Note, that despite the capacitor is placed on the opposite side as the MCU, this solution is the best.

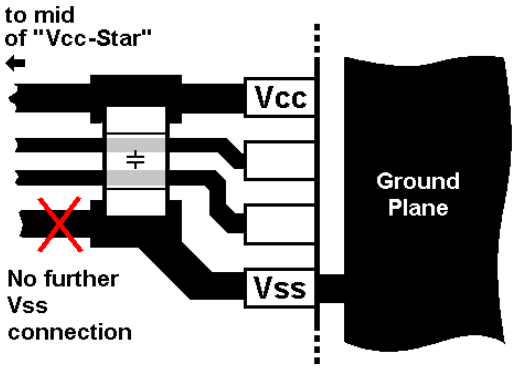


2.4 Power Supply Decoupling

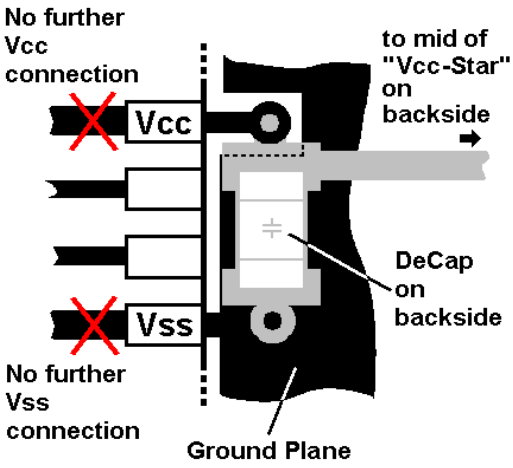
DeCaps for power supply have to be placed within the “current flow”. Otherwise they are senseless, because then their function become inoperable. The following graphic illustrates this:



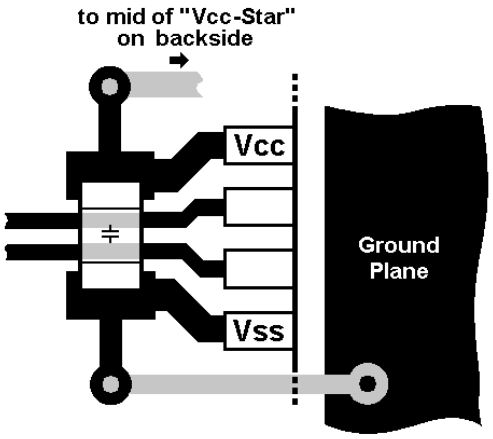
The following routing and placement for single sided metal layer is recommended:



The following routing and placement for double sided metal layer is recommended. Note, that despite the capacitor is placed on the opposite side as the MCU, this solution is the best like for the C pin.



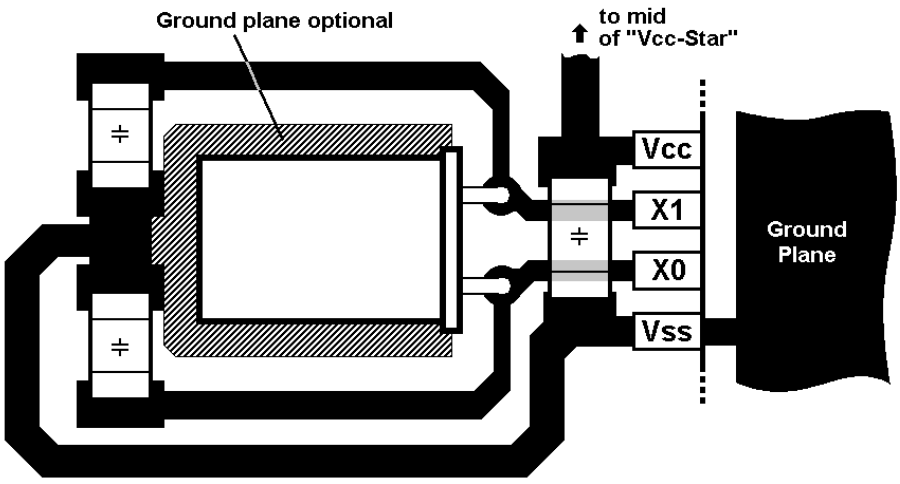
If mounting on both sides is not possible the following placement and routing is recommended:



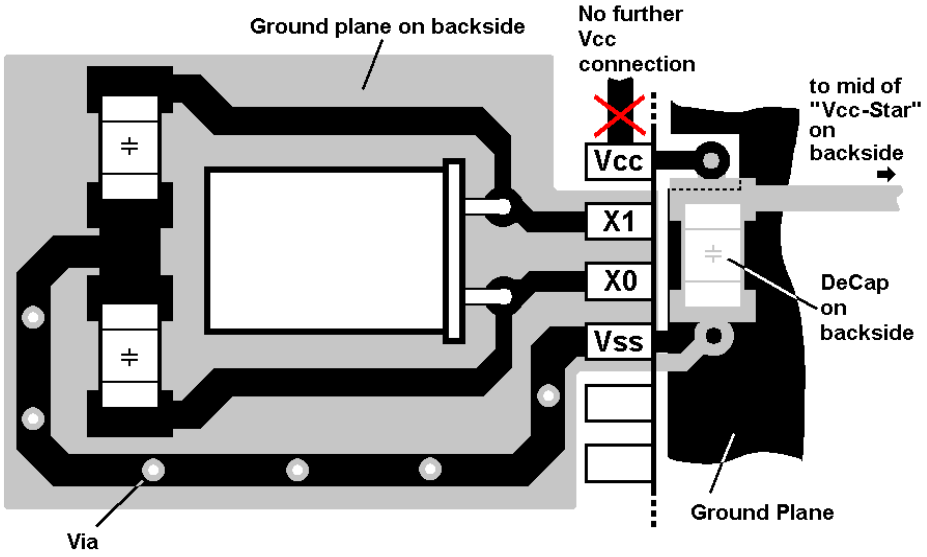
2.5 Quartz Crystal Placement and Signal Routing

The crystal has to be placed as nearest as possible to the MCU. Therefore the oscillator capacitors has to be placed “behind” the crystal.

For single metal layer circuit board the following placement and signal routing is recommended:



For double sided metal layer layout the following is recommended:



2.6 Other documents

For further detailed information please refer to the application note *16bit-EMC-Guideline*.

2.7 MCU Pin Summary

The following table shows the EMC critical pins and gives short information about how to connect them.

Pin name	Function
VCC	Main supply for IO buffer MCU core, close to input the internal 3.3V regulator, close to crystal oscillator
VSS	Main supply for IO buffer and MCU core, close to the internal 3.3V regulator, close to crystal oscillator
C	External smooth capacitor for internal 3.3V regulator output, it is used for supply of the MCU core. Note, that this pin leads the most of noise

AVCC*	Power supply for the A/D converter
AVSS*	Power supply for the A/D converter
AVRL*	Reference voltage input for the A/D converter
AVRH*	Reference voltage input for the A/D converter
DVCC*, HVCC*	Power supply for the PWM (high current) outputs, it is not connected to VCC, should be connected to extra power supply
DVSS*, HVSS*	Power supply for the PWM (high current) outputs, it is not connected to VSS, should be connected to extra power supply
X0, X0A*	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see please DS)
X1, X1A*	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1 pin, if not used so shall be open

*only if supported by device

3 Port Input / Unused Pins / Latch-up

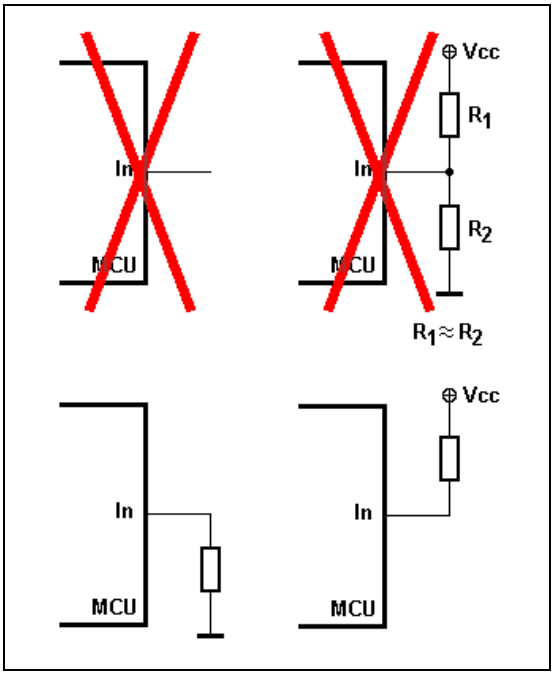
How to connect Input Port Pins and how to proceed with unused Pins

3.1 Port Input

It is strongly recommended to do not leave Input Pins unconnected. In this case those pins can enter a so-called *floating state*. At least this causes a high I_{CC} current. The worst case is a resulting latch-up effect that may defect the MCU.

Use the internal pull-up resistors, if the port provides such function. If not, use external pull-up or pull-down resistors to define the input-level. If both solutions are not possible, set the Port Pin to Output.

Never connect a potential divider with almost same resistor values.



Be careful with connection of input pins to other devices, which can go into High-Z states. Always use pull-up or pull-down resistors in this case.

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to chapter 3.3.

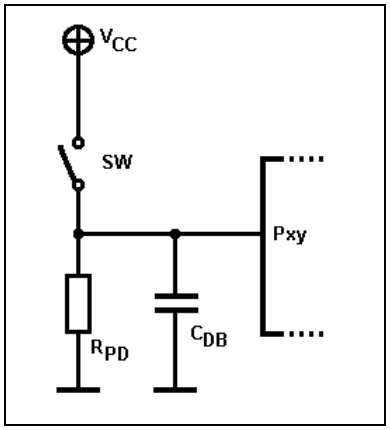
3.2 Unused Pins

All pins are set to input after its power-on default. Therefore set unused pins to output or provide them with pull-up or pull-down resistors.

3.3 Latch-up consideration

Be careful with external switches to V_{CC} or ground together with debouncing capacitors connected to port pins.

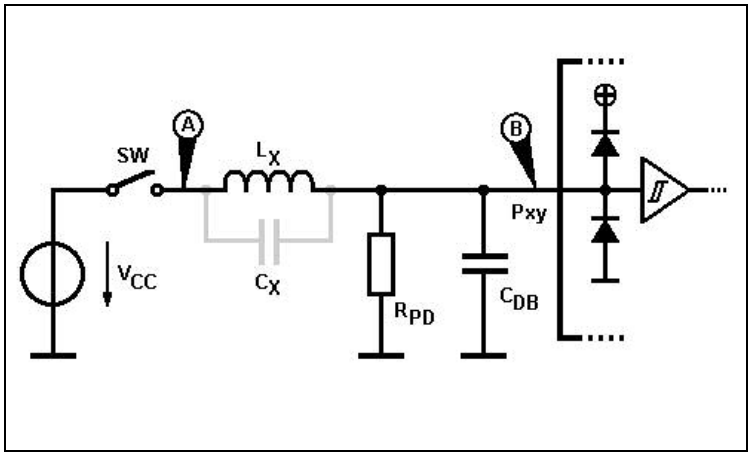
A usual configuration are shown in the following schematic:



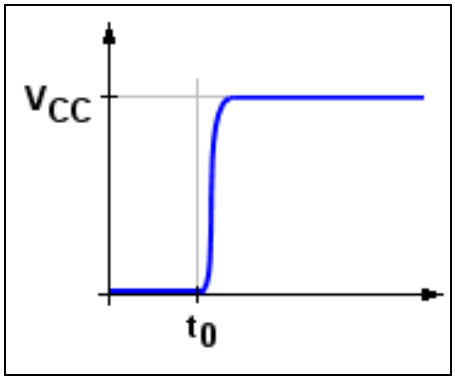
R_{PD} is a pull-down resistor and C_{BD} a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity L_X (and capacity C_X).

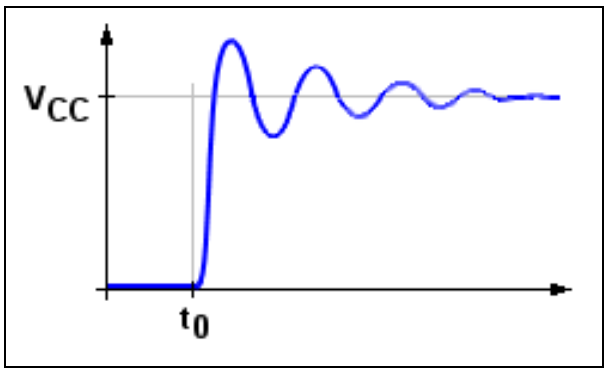
An equivalent circuit diagram looks like the following illustration:



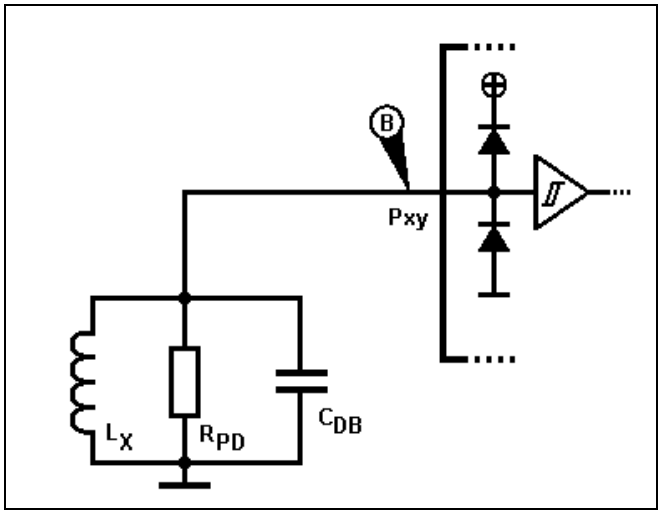
By closing the switch SW at time t_0 the following voltage can be measured at point (A):



But at the port pin Pxy on point (B) the following voltage can be measured:

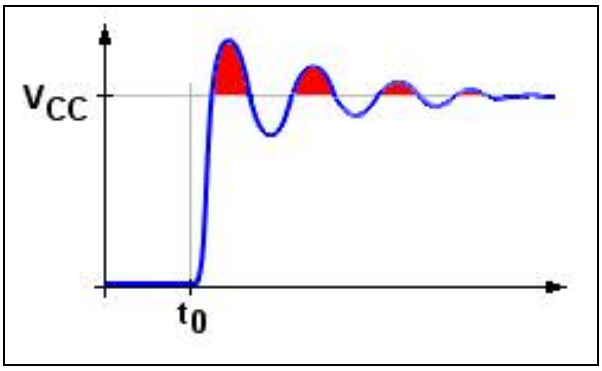


By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debouncing capacity C_X and the damping R_{PD} of the pull-down resistor (Assume the power supply to be ideal, i. e. it has no internal resistance):



Because R_{PD} is often chosen high (> 50 K Ohms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to V_{CC} becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are under shoots on the port pin.

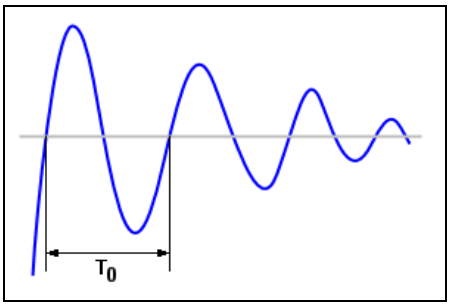
The frequency of the oscillation can be calculated by

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}} .$$

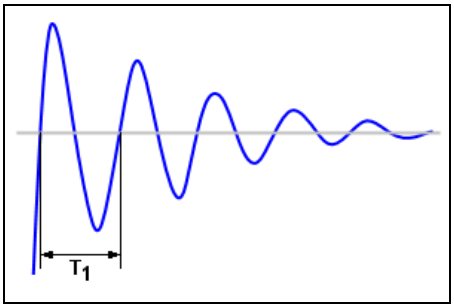
The inductivity L_X is the unknown value and depends on the PCB and the wire lengths.

There are two counter measurements to prevent from latch-up.

One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.



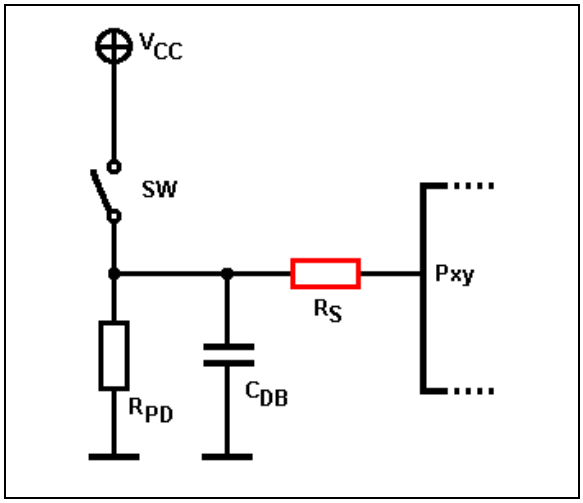
"big" capacity



"small" capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

A better solution is to use a series resistor at the port pin like in the following schematic:



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the CMOS level.