dsp28335 之 GPIO

注：本系列文章主要针对 TI 公司的 C28xx 系列 DSP 芯片的一些功能模块进行介绍，并描述基本的配置。文章中提到的 DSP 芯片未说明即默认为 TMS320F28335，简称为 28335。

GPIO（General-Purpose Input/Output）——通用输入/输出口，对大多数从事电子行业的人来说并不是什么陌生的东西。但它却是基础性的，很多 MCU 的后续开发都得用到 GPIO。

28335 有 88 个 IO 口，为 GPIO0 至 GPIO87，其中 GPIO0 至 GPIO63 可以配置为 8 个核心中断。28335 的 GPIO 口可以分为三组，分别为 A 口（GPIO0 至 GPIO31），B 口（GPIO32 至 GPIO63）和 C 口（GPIO64 至 GPIO87）。

GPIO 的寄存器可以分为三种，分别是 GPIO 控制寄存器，GPIO 数据寄存器和 GPIO 中断与低功耗模式选择寄存器。详见表 1、2、3。

GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
Reserved	0x6F8E – 0x6F8F	2	
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 63)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 47)
GPBQSEL2	0x6F94	2	GPIOB Qualifier Select 2 Register (GPIO48 to 63)
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 47)
GPBMUX2	0x6F98	2	GPIO B MUX 2 Register (GPIO48 to 63)
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 63)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 63)
Reserved	0x6F9E – 0x6FA5	8	
GPCMUX1	0x6FA6	2	GPIO C MUX1 Register (GPIO64 to 79)
GPCMUX2	0x6FA8	2	GPIO C MUX2 Register (GPIO80 to 87)
GPCDIR	0x6FAA	2	GPIO C Direction Register (GPIO64 to 87)
GPCPUD	0x6FAC	2	GPIO C Pull Up Disable Register (GPIO64 to 87)
Reserved	0x6FAE – 0x6FBF	18	

表 1：GPIO 控制寄存器

GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 63)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 63)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 63)
GPBTOGGLE	0x6FCE	2	GPIOB Data Toggle Register (GPIO32 to 63)
GPCDAT	0x6FD0	2	GPIO C Data Register (GPIO64 to 87)
GPCSET	0x6FD2	2	GPIO C Data Set Register (GPIO64 to 87)
GPCCLEAR	0x6FD4	2	GPIO C Data Clear Register (GPIO64 to 87)
GPCTOGGLE	0x6FD6	2	GPIO C Data Toggle Register (GPIO64 to 87)
Reserved	0x6FD8 – 0x6FDF	8	

表 2：GPIO 数据寄存器

GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE3	1	XINT3 GPIO Input Select Register (GPIO32 to 63)
GPIOXINT4SEL	0x6FE4	1	XINT4 GPIO Input Select Register (GPIO32 to 63)
GPIOXINT5SEL	0x6FE5	1	XINT5 GPIO Input Select Register (GPIO32 to 63)
GPIOXINT6SEL	0x6FE6	1	XINT6 GPIO Input Select Register (GPIO32 to 63)
GPIOINT7SEL	0x6FE7	1	XINT7 GPIO Input Select Register (GPIO32 to 63)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

表 3：GPIO 中断与低功耗模式选择寄存器

我们按照表中的寄存器的顺序来讲解。

GPIO 限制控制寄存器 GPxCTRL(x=A,B,C)为配置为输入限制的引脚指定了采样周期。

采样周期介于限制采样周期之内，是相对于系统时钟周期的倍数。具体的配置见表 4，以 A 口为例。

Bits	Field	Value	Description (1)
31-24	QUALPRD3		Specifies the sampling period for pins GPIO24 to GPIO31.
		0x00	Sampling Period = $T_{SYSCLKOUT}$ (2)
		0x01	Sampling Period = 2 × $T_{SYSCLKOUT}$
		0x02	Sampling Period = 4 × $T_{SYSCLKOUT}$
		. . .	. . .
		0xFF	Sampling Period = 510 × $T_{SYSCLKOUT}$
23-16	QUALPRD2		Specifies the sampling period for pins GPIO16 to GPIO23.
		0x00	Sampling Period = $T_{SYSCLKOUT}$ (2)
		0x01	Sampling Period = 2 × $T_{SYSCLKOUT}$
		0x02	Sampling Period = 4 × $T_{SYSCLKOUT}$
		. . .	. . .
		0xFF	Sampling Period = 510 × $T_{SYSCLKOUT}$
15-8	QUALPRD1		Specifies the sampling period for pins GPIO8 to GPIO15.
		0x00	Sampling Period = $T_{SYSCLKOUT}$ (2)
		0x01	Sampling Period = 2 × $T_{SYSCLKOUT}$
		0x02	Sampling Period = 4 × $T_{SYSCLKOUT}$
		. . .	. . .
		0xFF	Sampling Period = 510 × $T_{SYSCLKOUT}$
7-0	QUALPRD0		Specifies the sampling period for pins GPIO0 to GPIO7.
		0x00	Sampling Period = $T_{SYSCLKOUT}$ (2)
		0x01	Sampling Period = 2 × $T_{SYSCLKOUT}$
		0x02	Sampling Period = 4 × $T_{SYSCLKOUT}$
		. . .	. . .
		0xFF	Sampling Period = 510 × $T_{SYSCLKOUT}$

表 4：GPIO Port A Qualification Control (GPACTRL) Register Field Descriptions

而 GPIO 限制选择寄存器 GPxQSELy(x=A,B,C;y=1,2)指定了采样窗是 3 个采样点还是 6 个采样点。具体的配置见表 5，还是以 A 口为例。

Bits	Field	Value	Description (1)
31-0	GPIO15-GPIO0		Select input qualification type for GPIO0 to GPIO15. The input qualification of each GPIO input is controlled by two bits as shown in Figure 55.
		00	Synchronize to SYSCLKOUT only. Valid for both peripheral and GPIO pins.
		01	Qualification using 3 samples. Valid for pins configured as GPIO or a peripheral function. The time between samples is specified in the GPACTRL register.
		10	Qualification using 6 samples. Valid for pins configured as GPIO or a peripheral function. The time between samples is specified in the GPACTRL register.
		11	Asynchronous. (no synchronization or qualification). This option applies to pins configured as peripherals only. If the pin is configured as a GPIO input, then this option is the same as 0,0 or synchronize to SYSCLKOUT.

表 5：GPIO Port A Qualification Select 1 (GPAQSEL1) Register Field Descriptions

以上寄存器主要是为 GPIO 的输入功能进行的配置。通过，图 1（Qualification Using Sampling Window）和图 2（Input Qualifier Clock Cycles），我们可以很清楚的知道 GPIO 的输入限制是怎样完美的去除我们不需要的噪声的。

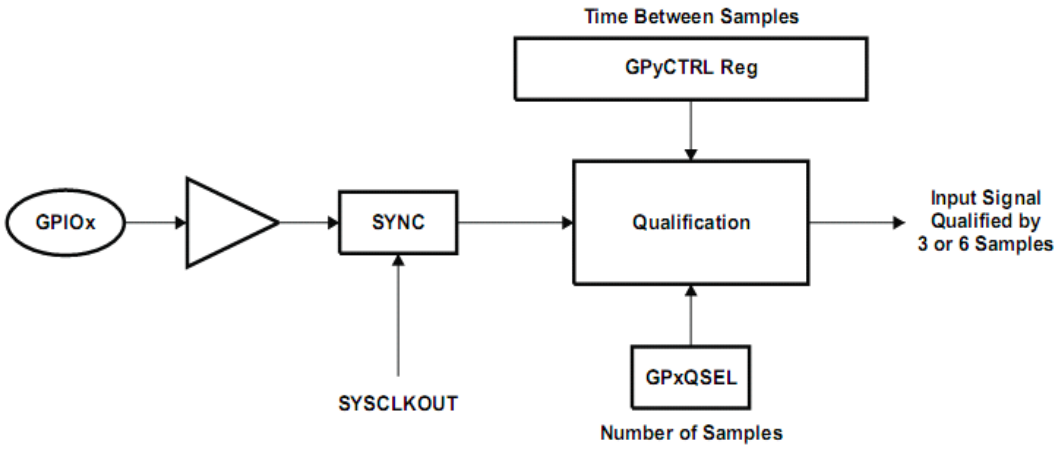

图 1：Qualification Using Sampling Window

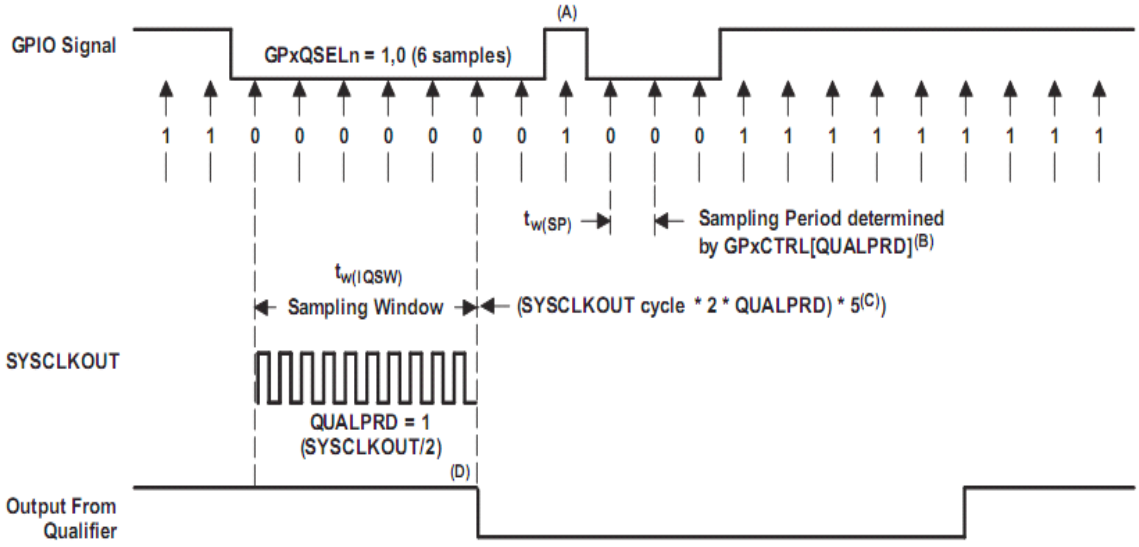

图 2：Input Qualifier Clock Cycles