DSPs Enhance Flexible Third-Generation Base-Station Design

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Designers are working on the third generation of cellular infrastructure equipment. This new equipment will give the service provider higher user capacity (translates to more revenue), but more importantly, the consumer gets access to high-speed data services, including wireless Internet access and wireless video transmission. With target data rates of 2 megabits per second, standards for this generation are in the process of being completed by the 3rd Generation Partnership Project (3GPP). Ability to deliver flexible systems is the critical key for equipment manufacturers to win in this market. Today's proposals talk of achieving 2 MB/s data rates, but what about the 10-MB/s data rates of tomorrow? Flexible designs will enable the systems that are deployed to grow with the demands of the consumer and the needs of the service provider.

Such flexibility in system design is of financial importance to service providers because it extends the time during which their investments in equipment are paying off. Over time, systems that are programmable and scalable with minimal board replacement reduce the total capital outlay for new services. In turn, equipment manufacturers reduce their overall engineering costs in systems that are flexible and scalable to meet the future demands of the service providers—the demand for continually increased capabilities at lower cost.

To the design engineer, flexibility means many things, including consideration of new technologies. The heart of the 3G systems is raw signal processing, both analog and digital. Technologies and techniques, such as direct intermediate-frequency (IF) sampling, direct digital down conversion, digital signal processing, and re-configurable logic, enable more flexible base station design options today than were available for second-generation (2G) systems. Using them, the design engineer can create infrastructure equipment that has the flexibility to support the needs of service providers, and has the performance and throughput to be scalable as infrastructure demand grows.

DSPs ARE ABUNDANT WITHIN THE 3G SYSTEM

Key base-station areas that require high-performance DSPs include:

- Antenna Arrays with Adaptive Digital Beam-Forming (BS)
- Power Control (BS)
- Voice Processing (BSC: Base-Station Control)
- Base Band Modem (BTS: Base Transceiver Station)

The algorithms employed in these functional blocks are MAC-intensive (i.e., they employ many steps of *multiply-and-accumulate*). MAC-intensive functions for 3G include FIR, correlation, and equalizer functions. The more rapidly these algorithms are performed, the better the quality and performance of a base station

The choice of a DSP to obtain the required computation speed is not a straightforward matter of specifying the highest clock speed. Architecture and instruction sets greatly affect the speed of algorithm execution. "MIPS" (millions of instructions per second) is also not a valid measure, since each manufacturer counts instructions differently. A highly useful recommended measure, more closely related to algorithm execution, is the peak *million-multiply-accumulates-per-second* (MMACS). This calculation is the product of the clock speed and the number of MACs the DSP is capable of executing per clock cycle[2].

Another aspect to consider is the class of DSP architecture employed. Two recently introduced new classes to consider are: *very long instruction word* (VLIW) and *static superscalar*.

VLIW attempts to reduce cost and increase execution speed by reducing hardware complexity. The sequencing mechanism in *VLIW* relies on an instruction format wherein every single execution unit in the chip is under direct programmer or compiler control. Unfortunately, VLIW has little or no hardware support for maintaining the integrity of data dependencies or avoiding scheduling hazards associated with real-time processing. In VLIW, all operation latencies in a particular implementation are fully exposed to software. The TMS320C6x series from Texas Instruments is an example of a VLIW architecture.

Static superscalar architectures enforce a consistent and functionally well-defined programming model, and the schedule is determined prior to run time. It incorporates static scheduling techniques like those found in VLIW, but it retains many superscalar and RISC attributes, enabling real time systems. Consequently, code can be written directly in assembly without requiring sophisticated timing prediction. The TigerSHARC™ DSP from Analog Devices is an example of a *static superscalar* architecture.

Antenna Arrays with Adaptive Digital Beam Forming

Digital beam-forming algorithms are designed to target source locations in a noisy environment. They rapidly compare responses of several spatially deployed antennas; the result of the computation is a signal that is believed to have originated from the target direction. Basically, they compute a correlation function that compares the signals and gives a measure of how close the desired and received signals are. Due to the many factors involved in the algorithm, and their wide dynamic range, floating point multiply-accumulate operations are used almost exclusively to minimize roundoff errors.

The target is mobile, and could be moving at a significant speed, this adds another dimension of complexity to the computation. *Adaptive beam-forming* makes use of additional information to continually track the mobile target. Beam-forming in 3G systems may be integrated with the Rake receiver, where the signal is operated on to combat fading and multipath effects. For these algorithms, the TigerSHARC's rapid performance of floating-point computations makes it an excellent fit.

TigerSHARC is a trademark of Analog Devices, Inc.

[1]Much of the material in this article first appeared in *Wireless System Design*, published by Penton Media, Inc., October, 1999, and in their Web version, http://www.wsdmag.com/, November, 1999.

[2]D. Efstathiou et al., "Recent Developments in Enabling Technologies for Software Defined Radio," *IEEE Communications* magazine, Aug., 1999.

[3]RT. Ojanpera, *Wideband CDMA for Third Generation Mobile Communications,* Boston-London: Artech House, 1998.

Power Control

In the code-division multiple-access (CDMA) systems proposed for 3G, base-station-initiated power control of remote-unit transmitters (uplink) is critical to compensate for fast fading, peaks in transmission power, and to avoid near-far problems[3]. This is necessary to reduce inter-cell interference. The computations required for power control are multiply-accumulate intensive, requiring high performance digital signal processing to meet delay time requirement in 3G systems.

Base stations may also implement the feedback mode transmit diversity (FMTD) algorithm, which is a power control/beam forming application that uses multiple antenna transmissions with varying weights. Again, the computation is multiply-accumulate intensive, similarly to the rake receiver. For such applications, the ADSP-21065L SHARC is a processor of choice.

Voice Processing

DSPs are the traditional choice for speech processing within the cellular system. The phone user's opinion of the quality of the system is directly dependent on the performance of the speech coder, and this has a strong influence on the channel density. Several speech coders are in use today in current 2G systems and must be supported in 3G systems. (See Table 1). Although lower codec bit rates increase equipment capacity, they worsen the speech quality. The critical DSP characteristics for high-quality voice processing combine large on-chip RAM and high processing capacity to support fast context switching and high channel density. The ADSP-21mod980, with its 8 DSP cores, capable of 600 MMACS (Million MACs per second), is the ideal candidate for this portion of the signal chain.

Table 1. Cellular Speech Codecs

Speech Codec	Bit Rate (Kbps)	Standard
QCELP	8	IS-95
EVRC	Variable	IS-95
ACELP	13	IS-95
VSELP	8	IS-136
GSM FR	13	GSM
GSM EFR	12.2	GSM
AMR	Variable	3G
GSM HR	5.6	GSM
JVSELP	8	PDC

Base Band Modem

The 3G standard is expected to be an essential factor that enables applications involving the transmission of wideband signals. Accordingly, the base band modem (BTS) must be designed and implemented with the ability to intermix high bandwidth applications and low bandwidth voice and paging. In the downlink, the base transceiver station packages parallel transport-block streams into physical channels; and in the uplink, it recreates the transport blocks from the base band signal.

Figure 2 shows a typical base band modem section of the 3G base station for both uplink and downlink configurations. During uplink, error-coding schemes are first applied to the transport block. Then the blocks are reordered and recombined with other channels before being sent off to the radio. For the downlink, the rake receiver is first used to sort out multipath effects and possibly to combine the data from several antennas. The blocks are then restored to their original order and channels before forward error correction is applied.

In the next section, the partitioning of the base band modem provides insight as to where a designer might choose to use a DSP. An optimum must be sought between minimizing the performance cost and maximizing the flexibility of the system to handle future design iterations.

BASE BAND MODEM PARTITIONING

Careful Partitioning for Maximum Flexibility

When deciding how to partition the modem, the nature of the algorithms and data rates become key factors in deciding what should be processed with an ASIC and what should be performed in the DSP. The next section describes some of these algorithms in detail, and explains the tradeoffs. This guideline depends upon the cost to process *N* channels of a specified bandwidth. For maximum flexibility, the entire structure could be implemented using a cluster of DSPs. On the other hand, a fixed specification may be most-economically implemented in an ASIC. When evaluating the most suitable approach, the flexibility criterion demands that an engineer consider how the design supports:

- quickly upgrading the parts of a system to newer technology,
- scaling the system to improve performance,
- product differentiation through the addition of new features.

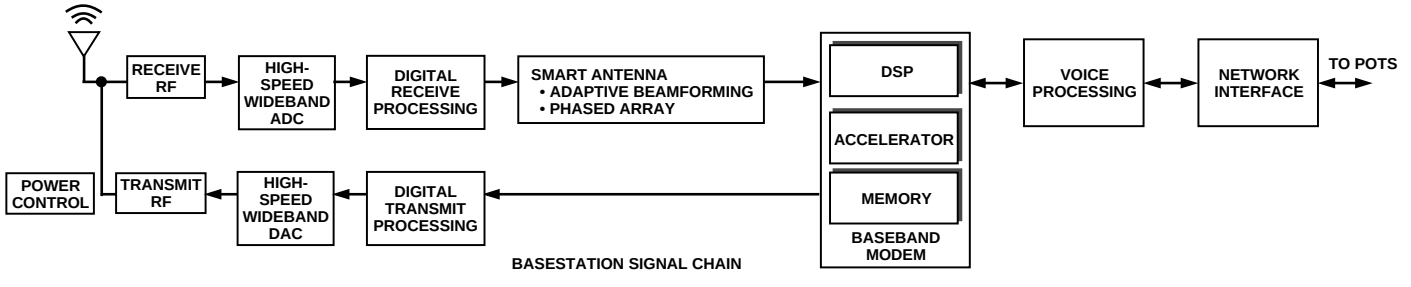

Figure 1. Where to find DSP technology in 3G systems.

Rake, Channel-Encoding/Decoding Hardware-Software Tradeoffs

Figure 2 shows different classifications for the different parts of the modem. Each of the blocks performs different types of computations. An overview is needed in order to see exactly where DSP is more appropriate than other alternatives.

The interleaving, channel segmenting, and rate matching are I/O-intensive operations, which combine data from several sources and reorganize data to minimize the effects of errors. Because of the variability of the parameters, data-rates, and memory-referencing, these functions are ideally suited to DSP for manipulation; they would be difficult to implement cost-effectively in an ASIC.

The error-coding and -correction algorithms involve significant bit manipulations that—properly implemented—can be implemented in the DSP. The error-correction algorithms also represent an area of the modem that can provide equipment-manufacturer differentiation. The encoding standards have been fixed, while decoding is left to implementers to design using their own intellectual property. Companies that have a strong ASIC capability might choose a hard-wired design, while others that are strong in programming and desire flexibility will choose the DSP approach. ADI's TigerSHARC DSP provides all the processing capacity to enable a single high speed 3G data channel.

3G systems, employing spread spectrum communications, will utilize CDMA spreading codes in order to provide greater use of available bandwidth. The spreading and despreading algorithms are multiply-accumulate intensive, but at extremely high data rates. The rake receiver takes its name from the fact that its diagram resembles a garden rake. Each finger tries to correlate the incoming data with the expected spreading code. As a result, the rake receiver needs to be able to process K times the determined bandwidth, where K is the number of fingers in the rake. In addition to that, the receiver must operate at the frequency set by the spreading codes.

DSP technology today doesn't cost-effectively support the bandwidth required for the spreading and despreading in 3G systems. However, production systems will not be manufactured and installed for several years, so there is every incentive for this situation to change. A clear examination of the upgrade path and projected performance of DSPs may show that, by the time these systems are deployed, these functions can indeed be handled cost-effectively.

Glueless Homogeneous and Heterogeneous Multiprocessing

Regardless of the technology used to implement each section of the base band modem, a significant amount of data must be moved around the system. In considering the design, components (or groups of components) that support high-bandwidth communications must be used. The TigerSHARC DSP provides several options for high-speed communication, including on-chip DMA (direct memory-access) and SDRAM support, along with dedicated user-programmable link ports. In multiprocessing designs, a high speed cluster bus can be used to connect as many as eight TigerSHARC DSPs without additional logic.

CONCLUSION

Designers of 3G base stations will make use of the DSPs in order to achieve the high performance and flexibility needed for tomorrow's voice and data applications. Flexibility at all levels will drive the need for scalable technologies, such as static super scalar architectures and glueless interconnection of system components. Effective embodiment of these design principles will fulfill the promise of 3G to provide the foundations of the kind of wireless infrastructure necessary for tomorrow's killer applications.

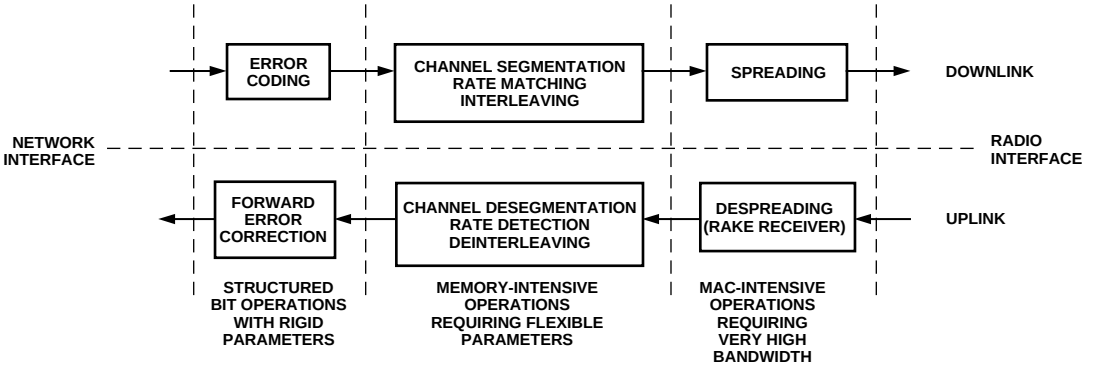

Figure 2. Block diagram showing the baseband processor's signal chain.