VX8812

HIGH DEFINITION VIDEO

TO

TV ENCODER

Headquarters Room B7, 1F, No.1, Li_Hsin Rd. I, Science Based Industrial Park, HsinChu City, 300, Taiwan, R.O.C. Tel : 886-3-5630888 Fax: 886-3-5630889		VXIS Technology Corp. http://www.vxis.com

Table of Contents

1 OVERVIEW

1.1 DESCRIPTION

VX8812 is an advanced high definition video to TV encoder coversion chip. It consists of video input format converter, picture enhancement and color processing, and the any ratio vertical and horizontal scaler, video output format converter and standard TV encoder.

It receives any format of input, such as RGB 24 -bit, YUV 24-bit, YUV 16-bit and YUV 8-bit or CMOS Bayer format raw data. It can also process sync embedded input such as bt-656 or bt-1120 format. The input resolution can be interlace such as 480i, 576i, 1080i or progressive such as 480P, 576P, 720P, 1080P, 4K2K.

The output format is standard TV NTSC or PAL analog output. There are three analog DAC output pin, it can be configured as CVBS+S-video output, or three CVBS output simultaneously or YPbPr output or RGB output. With the embedded frame buffer, the VX8812 can perform any input frame rate conversion to 50/60 Hz frame output for NTSC/PAL format.

The VX8812 can perform high quality picture enhancement such as video noise reduction, sharpening, black-level / white-level extension, gamma correction, and brightness, contrast, saturation, hue processing. There are also font-based on-screen-display (OSD), with 64 programmable font to make it suitable for different video application.

1.2 APPLICATION

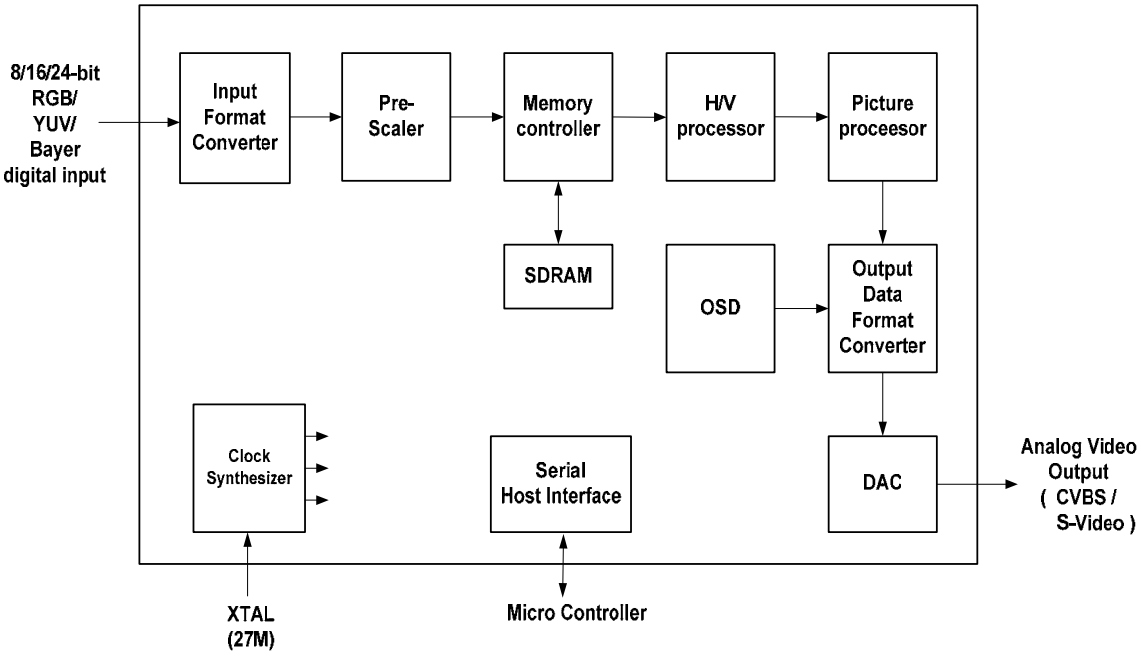
- Video format converter to TV
  (ex. HDMI/VGA to TV converter)
- Surveillance (Sensor to TV converter)
- Car/Multimedia panel
- Set-top box

1.3 FEATURES

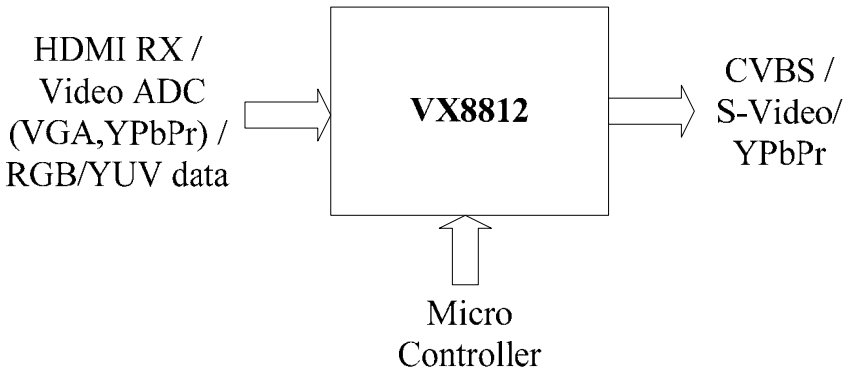
- Support Various Digital Video Input Formats
  - 8-bit interlace ITU-R BT.656
  - 8-bit progressive BT.656
  - 8-Bit ITU-R BT.601 + Horizontal Sync + Vertical Sync
  - 16-bit Y/UV input
  - 24-bit RGB/YUV progressive input
  - 8-bit CMOS Raw Bayer format input
  - BT.1120 16 bit input
- Resolutions of all input format are up to 1080P/4K2K
- Support three NTSC/PAL Analog output
  - 1 CVBS + 1 S(Y,C) Video output
  - 3 CVBS output
  - YPbPr SD output
  - RGB SD output
- Frame rate up/down conversion
- 3D noise reduction
- Video Flip, Mirror, Still
- Auto white balance
- Cross color suppression
- Embedded Scaling Engine (Relács), Supporting input Resolution from 320X240 to 1920X1080
- Brightness, Contrast, Saturation, and Hue Adjustment
- Color Transient Improvement, Adaptive Black-Level Extension, Skin Tone Enhancement.
- Frequency Directive Picture Sharpening
- 3-Channel 10-Bit Build-In Color gamma Look-Up Table for Video Fine-Tune
- Host Interface Compatible with Two-Wire IIC, Serial Interface
- OSD with 128 Build-in and 64 Programmable Font and Attribute Table, 16 Colors at same Time from 16,777,216-Color Template, Blinking, and Blending
- R/G/B input port swap & rotation control
- One 27MHz crystal needed
- 1.8V / 3.3V power supply with 3.3V digital I/O

1.4 BLOCK DIAGRAM

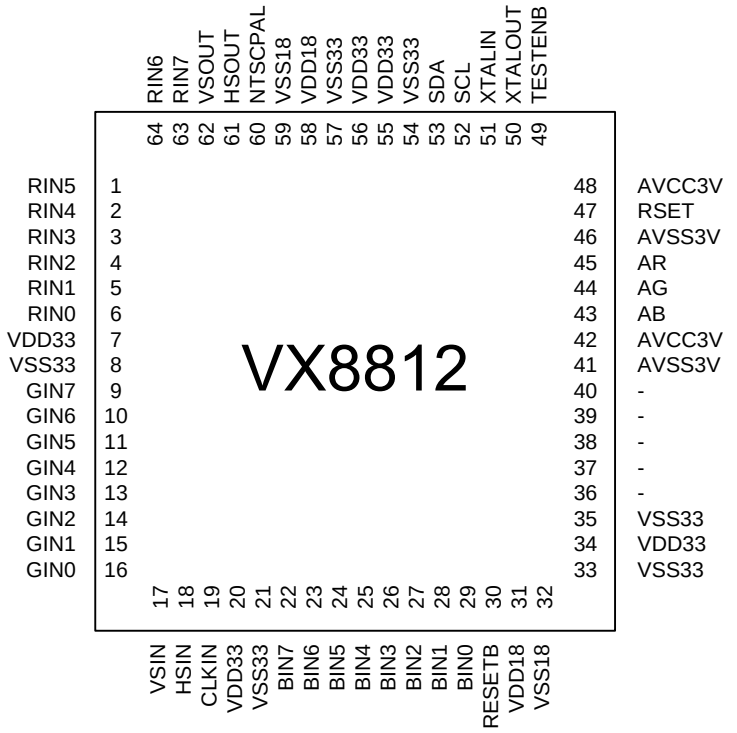
1.4.1 BLOCK DIAGRAM OF VX8812



1.4.2 APPLICATION OF VX8812



1.5 PINOUT DIAGRAM



1.6 PIN ASSIGNMENT

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	RIN5	17	VSIN	33	VSS33	49	TESTENB
2	RIN4	18	HSIN	34	VDD33	50	XTALOUT
3	RIN3	19	CLKIN	35	VSS33	51	XTALIN
4	RIN2	20	VDD33	36	-	52	SCL
5	RIN1	21	VSS33	37	-	53	SDA
6	RIN0	22	BIN7	38	-	54	VSS33
7	VDD33	23	BN6	39	-	55	VDD33
8	VSS33	24	BIN5	40	-	56	VDD33
9	GIN7	25	BIN4	41	AVSS3V	57	VSS33
10	GIN6	26	BIN3	42	AVCC3V	58	VDD18
11	GIN5	27	BIN2	43	AB	59	VSS18
12	GIN4	28	BIN1	44	AG	60	NTSCPAL
13	GIN3	29	BIN0	45	AR	61	HSOUT
14	GIN2	30	RESETB	46	AVSS3V	62	VSOUT
15	GIN1	31	VDD18	47	RSET	63	RIN7
16	GIN0	32	VSS18	48	AVCC3V	64	RIN6

1.7 PIN DESCRIPTION

Video Input Pins

Name	Type	Description	Notes
RIN7~0	I	Red input data	
GIN7~0	I	Green/BT656/Bayer input data	
BIN7~0	I	Blue input data	
VSIN	I	Input Vertical Synchronization	
HSIN	I	Input Horizontal Synchronization	
CLKIN	I	Input Data Clock	

Video Output Pins

Name	Type	Description	Notes
HSOUT	O	Video Output Horizontal Synchronization / GPO1	
VSOUT	O	Video Output Vertical Synchronization / GPO0	

Analog Video Output Pins

Name	Type	Description	Notes
AR	O	S-Video Y / CVBS / R analog output	
AG	O	CVBS / G analog output	
AB	O	S-Video C / CVBS / B analog output	
RSET	A	DAC gain control pin	

Miscellaneous I/O Pins

Name	Type	Description	Notes
RESETB	I_{PU}	Chip Reset (Active Low)	
XTAL_OUT	XO	Crystal Output	
XTAL_IN	XI	Crystal Input	
SDA	I_{PU}/O	Host Interface Serial Data / Address	
SCL	I_{PU}	Host Interface Serial Clock	
TEST_ENB	I_{PU}	Test Mode Enable (Active Low)	
NTSCPAL	I_{PD}/ O	CVBS NTSC/PAL output Select / Clock output	

Power Pins

Name	Type	Description	Notes
VDD33	P_{33}	Digital 3.3V power for I/O	Qty: 5
VSS33	G	Digital Ground For I/O	Qty: 6
VDD18	P_{18}	Digital 1.8V Power for Core	Qty: 2
VSS18	G	Digital Ground for Core	Qty: 2
AVCC3V	P_{33}	Analog 3.3V power for DAC	Qty: 2
AVSS3V	G	Analog ground for DAC	Qty: 2

note :	
I	3.3V input
O	3.3V output
I/O	3.3V input/output
I_{PU}	3.3V input with internal pull up
XI,XO	crystal input, output pin
P_{33}	3.3V power pin
P_{18}	1.8V power pin
G	Ground pin

1.8 PACKAGE

- VX8812 64-Pin LQFP

2 VIDEO I/O PIN ASSIGNMENT

2.1 DIGITAL VIDEO INPUT ASSIGNMENT

The VX8899 digital video interface is compatible with extensive digital video output standard formats mostly used by current video transmission methods. As for input, VX8899 directly supports interlaced 8-bit YUV with (ITU-R BT.656) or without (ITU-R BT.601) embedded synchronization, It also supports progressive 8-bit YUV input and 16-bit Y/UV, 24-bit YUV, 24-bit RGB input or progressive CMOS Bayer format, and interlace 1080i(BT.1120) format.

The pin arrangement for each format is defined in *Table 2.1.*

Table 2.1 Digital Video Input Pin Assignment

Pin Name	I/O Type	Digital Input			
		8-bit YUV	16-bit YUV	24-bit YUV	24-bit RGB
RIN [7]	**I**	-	UV[7]	V[7]	R[7]
RIN [6]	**I**	-	UV[6]	V[6]	R[6]
RIN [5]	**I**	-	UV[5]	V[5]	R[5]
RIN [4]	**I**	-	UV[4]	V[4]	R[4]
RIN [3]	**I**	-	UV[3]	V[3]	R[3]
RIN [2]	**I**	-	UV[2]	V[2]	R[2]
RIN [1]	**I**	-	UV[1]	V[1]	R[1]
RIN [0]	**I**	-	UV[0]	V[0]	R[0]
GIN [7]	**I**	YUV [7]	Y[7]	Y[7]	G[7]
GIN [6]	**I**	YUV [6]	Y[6]	Y[6]	G[6]
GIN [5]	**I**	YUV [5]	Y[5]	Y[5]	G[5]
GIN [4]	**I**	YUV [4]	Y[4]	Y[4]	G[4]
GIN [3]	**I**	YUV [3]	Y[3]	Y[3]	G[3]
GIN [2]	**I**	YUV [2]	Y[2]	Y[2]	G[2]
GIN [1]	**I**	YUV [1]	Y[1]	Y[1]	G[1]
GIN [0]	**I**	YUV [0]	Y[0]	Y[0]	G[0]
BIN [7]	**I**	-	-	U[7]	B[7]
BIN [6]	**I**	-	-	U[6]	B[6]
BIN [5]	**I**	-	-	U[5]	B[5]
BIN [4]	**I**	-	-	U[4]	B[4]
BIN [3]	**I**	-	-	U[3]	B[3]
BIN [2]	**I**	-	-	U[2]	B[2]
BIN [1]	**I**	-	-	U[1]	B[1]
BIN [0]	**I**	-	-	U[0]	B[0]

2.2 ANALOG VIDEO OUTPUT ASSIGNMENT

The VX8812 has three analog video output pins “AR”,”AG”,”AB”. Different analog video format can be output to these pins, such as RGB format, YPbPr format, S-video Y/C format or CVBS format. But the output resolution of these format is just 480i or 576i. The different output format can be assigned by setting the register “OUTFMT”(register address 0xC0[7:6]) value.

These format setrting are shown in *Table 2.2*

OUTFMT	AR	AG	AB
0	R	G	B
1	PR	Y	PB
2	SVIDEO_Y	CVBS	SVIDEO_C
3	CVBS	CVBS	CVBS

Table 2.2 Analog Video Output Pin Assignment

When the output format is CVBS, the different TV standard for NTSC/PAL can be selected by setting the register “TVSTD”(register address 0xC0[1:0]). As shown in *Table 2.3*

TVSTD	NTSC	PAL
0	NTSC-M	PAL-B,G,D,H,I
1	NTSC-J	PAL-N
2	PAL-M	PAL-Nc
3	-	-

Table 2.3 Analog Video Output Pin Assignment

The three channel output can also be swaped by setting register “POUT_RGB_MUX(register address 0x7F[2:0]), as shown in *Table 2.4*

OUT_RGB_MUX	R	G	B
0	R	G	B
1	B	G	R
2	G	R	B
3	B	R	G
4	G	B	R

5	R	B	G
6	G	G	G
7	R	R	R

Table 2.4 Analog Video Output Pin Assignment

3 CLOCK SYSTEM

3.1 REFERENCE CLOCK

There is one crystall needed for VX8812, the input crystall frequency is 27MHz. The PLL frequency is set by registers PLL_OD1, PLL_NR1,PLL_NF1 in register addres 0x06,0x07,0x08, and the formula is shown in Eq. 3.1

$$PLLOutputFrequency = PLLInputFrequency \times \frac{(PLL\_NF+1)}{(PLL\_NR+1)} \times \frac{1}{(PLL\_OD')} \times \frac{1}{(PLL\_DIV+1)}$$

Where PLL_OD' = 1, when PLL_OD1 = 0. PLL_OD' = 2, when PLL_OD1 = 1,
PLL_OD' = 4, when PLL_OD1 = 2. PLL_OD' = 8, when PLL_OD1 = 3,

Eq. 3.1 PLL frequency calculation

The PLL output clock is used for SDRAM read/write control.
The output clock is only 27MHz for video encoder output.

4 HOST INTERFACE

The VX8812 host interface uses two-wire IIC compatible interface protocol, one for clock, and one for multiplexed data/address. Input pin SCL is used for host clock input while input/output pin SDA is for multiplexed host data and address signal.

The chip write address is 0x12, as

0	0	0	1	0	0	1	0

The chip read address is 0x13, as

0	0	0	1	0	0	1	1

Once chip write and read addresses are configured, the host command byte sequence can be transfer to VX8812 via the serial interface. The byte sequence consists of a CHIP ADDRESS, a REGISTER ADDRESS, followed by a number of DATA BYTES. The CHIP ADDRESS and REGISTER ADDRESS must be always provided by the host, usually a micro-controller, and the DATA BYTES are provides by host for host-writings and by VX8812 for host-readings.

Fig 4.1 Host command write sequence

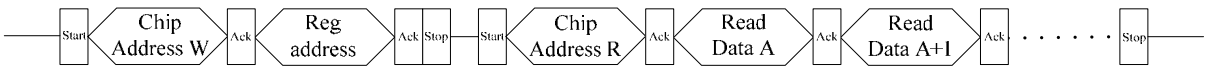


Fig 4.2 Host command read sequence

As shown above, the first DATA BYTE following REGISTER ADDRESS A is assigned or read to/from register address A, the DATA BYTE behind will be assigned/read to/from register address A+1, and so on. So for large host-writings such as chip initialization, only the initial register address needs to be specified once to complete whole host writing operations. In this manner user can save a lot of host command cycles in complicated applications.

5 HARDWARE AND SOFTWARE RESET

VX8812 can be reset to initial status in two ways. One is through the hardware pin, RESETB; by asserting RESETB pin to ground voltage, entire chip will be reset to its initial states. The other way is through the host interface by writing to register RST1 (01h). Writing value 5Ah to RST1, called software reset, will generate an internal reset pulse signal similar to RESETB to initialize the entire chip.

Similar to writing 5Ah to RST1, writing A5h to RST1 will reset entire chip *except* control registers programmed by host interface. The use of A5h writing often occurs after initial register programming or mid-state register changes to assure the chip working from the initial state.

6 VIDEO INPUT SELECTION

The VX8812 accepts 6 types of digital video formats as input data stream, it can be set by changing the value of register INFMT(address 0x10[2:0]). Following Table 6.1 shows VX8812's acceptable digital video input formats. For their pin assignment, please review *CHAPTER 2 DIGITAL VIDEO I/O PIN ASSIGNMENT*.

Table 6.1 Digital Video Input Format Selection

INFMT [2:0]	Digital Video Input Format
000	24-bit RGB progressive input
001	16/18/24-bit Y/U/V 4:4:4 input data
010	16-bit Y/UV 4:2:2 data
011	8-Bit ITU-R BT.656/BT.601
100	8-bit CMOS raw data Bayer format input
101	Reserved
110	Reserved
111	Reserved

The VX8812 accepts any data format of 24bit RGB/YUV, 16-bit Y/UV, 8-bit YUV with or without external sync. It will detect the external sync first from the input pin HSIN,VSIN. If no signal on these two pins, then sync header inside the data(like bt.656 or bt.1120) will be checked and extracted the horizontal and vertical sync. If no header found inside the data and no external sync in the sync pins, then it will be detcted as no video input, and register NO_VIDEO(address 0x1B[0]) will be 1.

The Vx8812 also can detect the input video resolution automatically. The detected resolution is from 480i to 1080P, and the detected mode can be check by reading register IMODE(address 0xE9[2:0])
The IMODE value corresponding to the resolutuon is shown as *Table6.2*

IMODE	0	1	2	3	4	5	6
RESOLUTION	480I	576I	480P	576P	720P	1080I	1080p

Table 6.2 Input Resolution Detected

The detected input horizontal length and active data, vertical total line number and active line number are shown in the register HSIN_LENGTH, HSIN_ACT, VSIN_LEBGTH, VSIN_ACT (address 0xE0~0xE5).

The input video frame rate information also can be calculated from the register FRAME_CNT(address 0xE6~0xE8). You can calculate the frame rate from the following equation :

Clocks number of 1 frame = FRAME_CNT[23:0] * 10
Frame rate = 27M / Clocks number of 1 frame

The input video horizontal active length and active line number are auto deteted and processed. If you want to set the video active horizontal width and vertical length manually, you can set the register MIL_EN(address 0x11[7]) = 1. Then you can set the active width by setting register M_HACT(address 0x12~0x13), and the active length by setting register M_VACT(address 0x12, 0x14).
You can also shift the active video data to left/right or up/down by setting the register VIHS_OFST(address 0x15,0x16), VIVS_OFST(address 0x15,0x17).

The VX8812 also supports DDR input mode, by setting register DDRIN_EN(address 0x18[5]), which latches the data in both the rising edge and falling edge of input clock.

7 PRE-SCALER

The pre-scaler do the scaling down on both vertical and horizontal direction for the input video.
The horizontal scaling down is set by the register PRE_SF_H(address 0x22), the value 0 means no scaling in the horizontal direction. The larger the PRE_SF_H value, the smaller the horizontal size. When the value equal to 0x80, the horizontal size is one half of the original size. If you want to scale down the horizontal szie more than 1/2 of the original size, set the value of PRE_H_SK(address 0x24[3:0]), the horisontal size will directly shrink to 1/(PRE_H_SK+1) of original size.

The vertical scaling down is set by the register PRES_SF_V(address 0x20,21), the value 0 means no scaling in the vertical direction. The larger the PRES_SF_V value, the smaller the vetrical size. When the value equal to 0x8000, the vertical size is one half of the original size. If you want to scale down the vertical size more than 1/2 of the original size, set the value of PRE_V_SK(address 0x24[7:4]), the vertical size will directly shrink to 1/(PRE_V_SK+1) of original size.

The active horizontal and vertical size after scaling down can be checked by reading the register PRE_HACT(address 0x26, 0x27), PRE_VACT(address 0x28,0x29).

A deflicker function is present to remove the flicker condition of interlace output. This function can be enabled by setting the register DEFLICKER_ON(address 0x25[7]), and the corresponding coefficient DEFLICK_COEFF(address 0x25[6:2]) for the deflicker effect.

8 COLOR ENHANCEMENT

8.1 CONTRAST, BRIGHTNESS, COLOR, AND HUE ADJUSTMENT

The VX8812 supports essential color adjustment through the registers, BRIGHTNESS, CONTRAST, SATURATION (address 0x31,0x32,0x33). The value 0x80 is no adjustment to the original video color. The Hue(address 0x34) is used to adjust the color of the video, the value 0x20 is no adjustment to the color.

The BRIGHTNESS and CONTRAST can also be adjustmented independently in color domain R,G,B by setting registers R_BRIGHTNESS, G_BRIGHTNESS, B_BRIGHTNESS(address 0x3B, 0x3C, 0x3D), and registers R_CONTRAST, G_CONTRAST, B_CONTRAST(address 0x3D, 0x3E, 0x3F).

8.2 BLACK-LEVEL EXTENSION (BLE)

Basic idea of black level extension is to enhance the contrast of the luminance in the dark potion of the picture. As the result, the average luminance in the dark potion will be extended to darker level non-linearly while the luminance in bright potion remains unchanged. The advantage of this function is to make the object more solid, apparent, and noticeable to the viewers. The BLE function works adaptively, depending on the average luminance of the picture.

8.3 VIDEO NOISE REDUCTION (VNR)

The VX8812 contains video noise reduction (VNR) engine specifically removing Gaussian noise and mid-band interception noise, which commonly occurs in video transmission channels. *Figure 10.3.1* shows the block diagram of VX8812's VNR engine. VNR function is enabled from the register VNR.

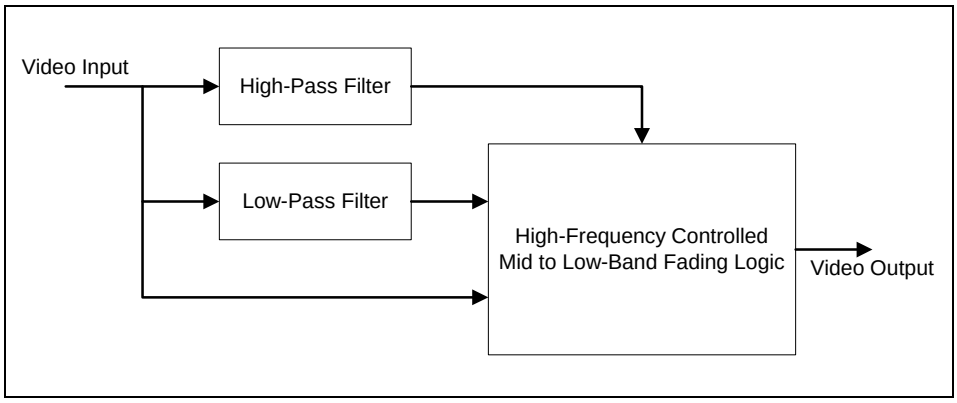


Figure 8.3.1 VX8812 VNR Engine Block Diagram

8.4 SHARPNESS

The VX8812 offers three peaking filters for different frequency response in horizontal sharpness engine. The gain for each filter is adjustable from 0 to 14 dB and individually controlled with registers, PEAK_ADJ1, PEAK_ADJ2, and PEAK_ADJ3. For peaking filter 1, 2, and 3, each respectively amplifies 1/2, 1/4, and 1/6 of sampling frequency (27 MHz). *Figure 8.4.1* illustrates the frequency response for each filter. Following the three peaking filters is a clipping filter to suppress video gain after peaking filters and reduce noise. The clipping filter is adjustable with the registers PEAK_CLIP_MIN and PEAK_CLIP_MAX. If the input value (summed gain) of the clipping filter is smaller than PEAK_CLIP_MIN, the output value of the clipping filter is clipped to zero. If the input value is between PEAK_CLIP_MIN and PEAK_CLIP_MAX, the output value of the clipping filter is linearly (input value - PEAK_CLIP_MIN). If the input value is larger than PEAK_CLIP_MAX, the output value of the clipping filter is clipped to (PEAK_CLIP_MIN - PEAK_CLIP_MAX).

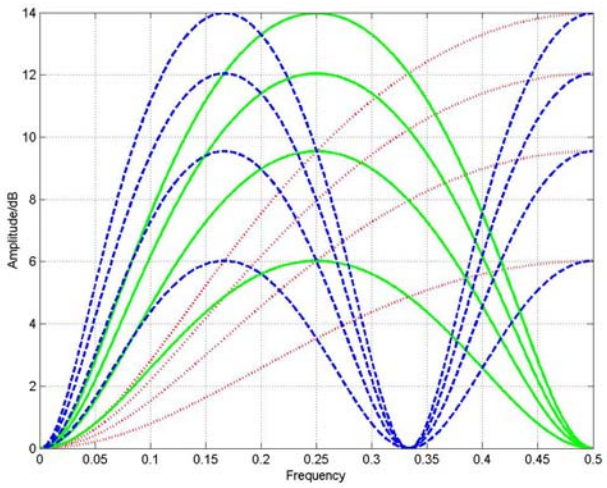


Figure 8.4.1 Frequency Response for Peaking Filters

8.5 COLOR-TRANSIENT IMPROVEMENT (CTI)

For most video solutions, video content in chrominance domain are often with less care due to human eye's neglect of color variations. Therefore, we sometimes found that the picture is implicitly dirty and

foggy especially when we observing the video patterns or color-bars. The color-transient improvement (CTI) engine in VX8812 is made to recover this imperfectness of video presentation and perform sharp and keen edges for every objects and overall clearer video to the viewers.

8.6 COLOR LOOK-UP TABLE (CLUT) AND GAMMA CORRECTION

The VX8812 provides method to finely manipulate video sequence, color look-up table (CLUT). CLUT is made of three embedded SRAMs and requires initial SRAM programming with continuous-write scheme of host interface. Register CLUT_MODE enable the usage of CLUT.

8.6.1 CLUT

Widely used in many applications, the VX8812 equips a build-in 3-channel 10-bit color look-up table (CLUT). The CLUT contains three 256 x 10-bit SRAMs, one for each of R/Pr, G/Y, and B/Pb channels. For each channel, the SRAM acts as an one-to-one mapping array and reads 8-bit data as index, and maps into 10-bit data as SRAM data output. By manipulating every single cell of SRAMs, user can make neat changes of the color mapping for each single level of 256 color levels in each channels. Using the CLUT, all the picture/video related adjustments such as color adjustment, gamma, and color temperature can be accomplished with specifically programmed mapping data. CLUT_MODE and the datawidth register CLUT_WIDTH, must be set before using the CLUT.

Programming the CLUT is intuitive through the continuous-write registers. First, program the destination SRAM to one or all of the R/Pr, G/Y, B/Pb channels with the register CW_DEST. Next, write the initial 8-bit address to register CW_INIT_ADDR. Then, in sequence write the data into the register CW_DATA, and the internal host interface controller will automatically write this data into the designated SRAM after a short period of time, and increment the address by 1 after each internal SRAM writing. If the CLUT data width is set to 10-bit, then the internal automatic SRAM writing operation will take place at every two host writing of CW_DATA (*Figure 8.6.1.1*).

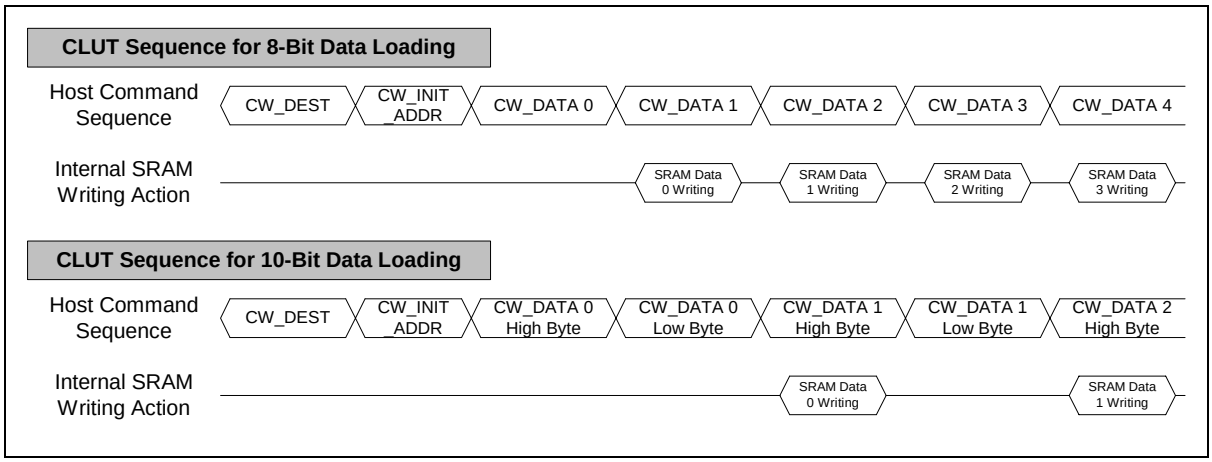


Figure 8.6.1.1 CLUT Programming Sequence Through Host Interface

Note that the CLUT always maps the video in the color domain of analog output port. This means when the analog output port is set to RGB, CLUT mapping is in RGB domain, and when the analog output is set to YPbPr or YUV, CLUT mapping is in YPbPr or YUV domain. Also, as shown in *Figure 8.6.1.2* that the value stored in the SRAM can be in 10-bit range (CLUT_WIDTH = 1), or in 8-bit range (CLUT_WIDTH = 0) in RGB or YUV domain mappings. But note that due to synchronization insertion to Y channel, in YPbPr domain CLUT only supports 8-bit mappings.

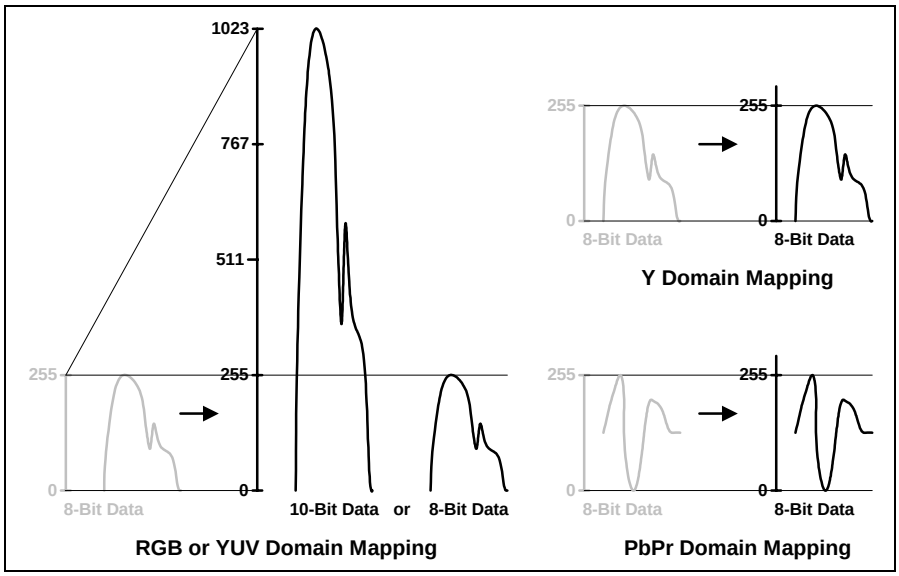


Figure 8.6.1.2 CLUT Mapping

9 POST-SCALER

The post-scaler is used to scale up the horizontal and vertical size of the video. This function is enabled by setting register POST_EN(address 0xA3[7]). The scaling coefficients in horizontal and vertical direction are controlled by register POST_SF_H(address 0xA2), POST_SF_V(address 0xA0,0xA1).

10 MEMORY CONTROLLER

There is a sdram embedded in the VX8812 for frame buffer processing. The memory access frequency is controlled by the PLL output as defined in the Eq.3.1. The clock phase can be adjusted by the register MCLK_DELAY(address 0x9B[7:4]), and the frame size in the frame buffer is set by the registers MCT_HLEN, MCT_HACT(address 0x93~0x95), MCT_VLEN, MCT_VACT(address 0x96~0x98).

The VX8812 also supports the video flip and mirror function. This can be done by setting the registers MIRROR_V, MIRROR_H.

A 3D noise reduction is also supported to reduce the video noise. The noise reduction function can be enabled by setting the register TNR_EN(address 0xA6[6]).

11 VIDEO OUTPUT DISPALY

Two essential elements, screen shifting and masking, control the VX8812 video output display. The screen shifting function is activated by changing the horizontal shifting register HSHIFT, and vertical shifting register VSHIFT. Setting larger value of HSHIFT moves the picture rightward; and setting larger value of VSHIFT moves the picture downward. Also, the screen masking function is activated by setting the registers BOTTOM_MASK, TOP_MASK, LEFT_MASK, and RIGHT_MASK. The VX8812's output display region with its synchronization and control parameters (screen shifting and screen masking) is summerized in *Figure 11.1*.

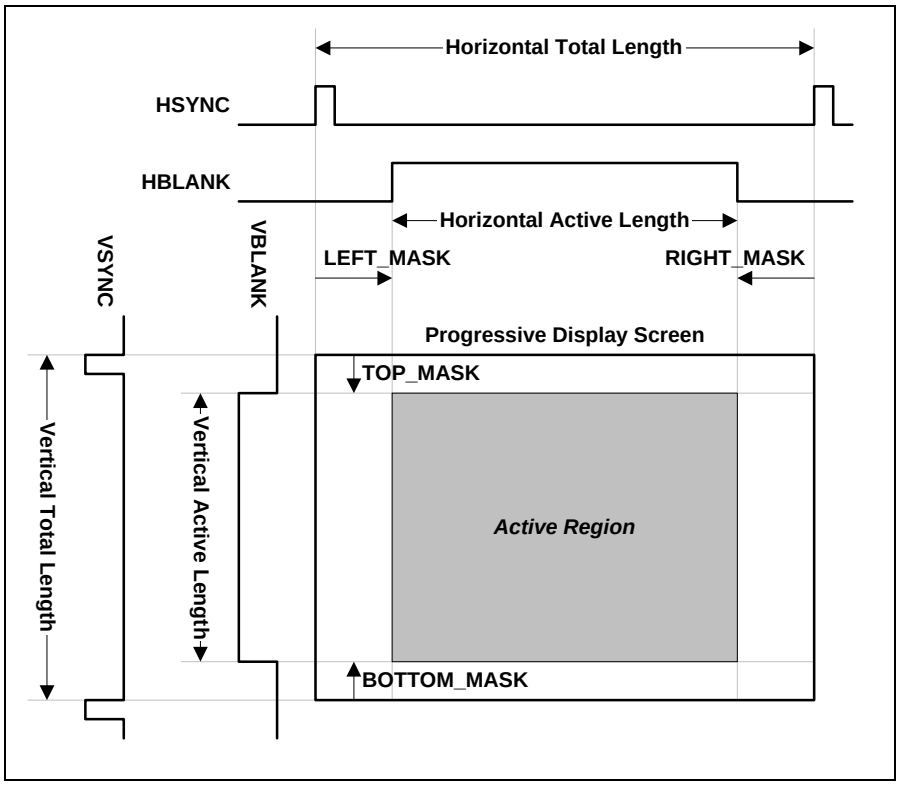


Figure 11.1 Output Display Region

12 ON-SCREEN-DISPLAY (OSD)

12.1 OSD INTRODUCTIONS

The VX8812 integrates VXIS's font-attribute-based on-screen display (OSD) unit, which can display a total of up to 256 characters in a single screen, with each font in 16 pixels x 20 pixels format. The embedded font Random-Access-Memory (RAM) and Read-Only-Memory (ROM) let user select characters from up to 192 fonts, 128 build-in and 64 programmable fonts. The attribute bits programming let user designate arbitrary spectacular menu, closed caption, even games from 16,777,216 colors, blinking, *Italic* font, underline font, and many artistic features.

12.2 OSD DISPLAY BLOCKS

The build-in OSD system divides the screen display into three basic sections, the title, content, and bottom blocks, and the user can customize the size and position for each display block by host commands (*Figure 12.2.1*).

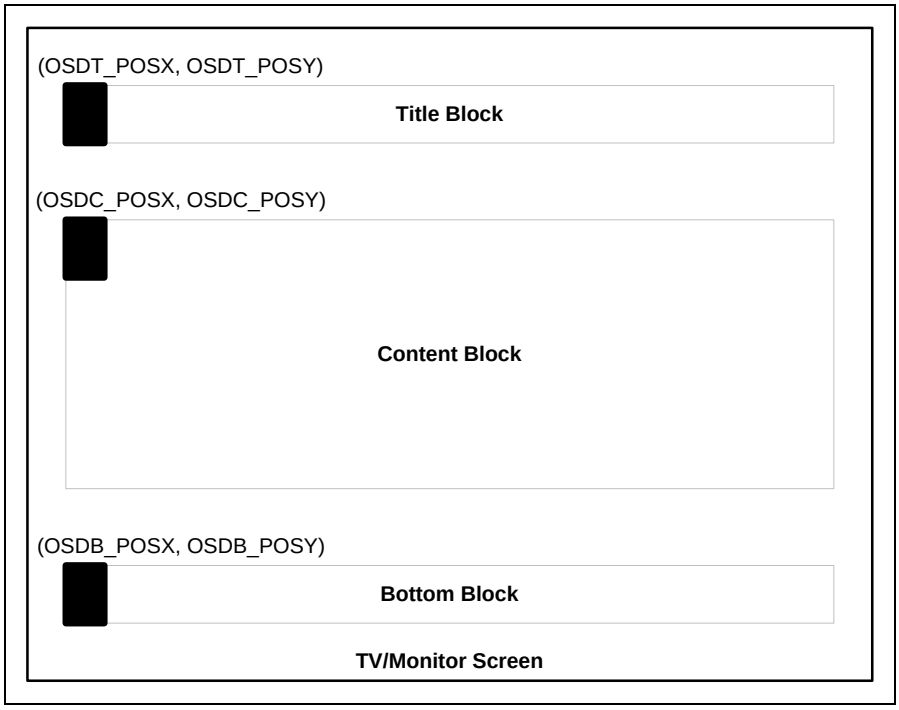


Figure 12.2.1 OSD Display Blocks

The title and bottom blocks are restricted to display one line of text commonly for header or page notes;

and the content block displays multiple lines of text for main OSD information. The sizes and the positions for each individual block are adjustable through registers (*Table 10.2.1*). Each displaying block cannot be overlapped with others. For details of the register setting, check OSD section in register description chapter.

Table 12.2.1 Position and Size Registers

Register		Description
OSDT_POSX	OSDT_POSY	Position registers for title block
OSDC_POSX	OSDC_POSY	Position registers for content block
OSDB_POSX	OSDB_POSY	Position registers for bottom block
OSDT_SIZEX	N/A	Size registers for title block
OSDC_SIZEX	OSDC_SIZEY	Size registers for content block
OSDB_SIZEX	N/A	Size registers for bottom block

12.3 OSD OPERATIONS

The VX8812's OSD unit is font-based entry. All information that is going to be shown in the screen must be translated into fonts, which is in 16 pixel x 20 pixel resolution each, then put into the screen.

There are two types of OSD memories embedded in VX8812. One is called the "font memory", which stores all the fonts currently being used on the screen. The font memory consists of one 128-font ROM (2560 x 16-bit) for commonly used fixed fonts, and one 64-fonts RAM (1280 x 16-bit) for user-programmable fonts (*Table 10.3.1*). If utilizing maximum amount of the memory, there are up to 192 fonts can be repeatly shown in the single page.

Table 12.3.1 Font Memory Table

Index (Hex)	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Character	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
Index (Hex)	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh
Character	Q	R	S	T	U	V	W	X	Y	Z	a	b	c	d	e	f
Index (Hex)	20h	21h	22h	23h	24h	25h	26h	27h	28h	29h	2Ah	2Bh	2Ch	2Dh	2Eh	2Fh
Character	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v
Index (Hex)	30h	31h	32h	33h	34h	35h	36h	37h	38h	39h	3Ah	3Bh	3Ch	3Dh	3Eh	3Fh
Character	w	x	y	z	á	à	â	ç	é	è	ê	í	î	Ñ	ñ	ó

Index (Hex)	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh
Character	ô	ú	û	!	,	.	;	:	'	"	#	%	&	@	/	(
Index (Hex)	50h	51h	52h	53h	54h	55h	56h	57h	58h	59h	5Ah	5Bh	5Ch	5Dh	5Eh	5Fh
Character	)	[	]	+	−	÷	<	=	>	?	°	¢	$	£	®	™
Index (Hex)	60h	61h	62h	63h	64h	65h	66h	67h	68h	69h	6Ah	6Bh	6Ch	6Dh	6Eh	6Fh
Character	½	¿	0	1	2	3	4	5	6	7	8	9	♪			■
Index (Hex)	70h	71h	72h	73h	74h	75h	76h	77h	78h	79h	7Ah	7Bh	7Ch	7Dh	7Eh	7Fh
Character	▔	▏	▎	▍	▌	▋	▊	▉	▉	^	v	▔	_	▕	▕	□
Index (Hex)	80h	81h	82h	83h	84h	85h	86h	87h	88h	89h	8Ah	8Bh	8Ch	8Dh	8Eh	8Fh
Character	User-Programmable Fonts															
Index (Hex)	90h	91h	92h	93h	94h	95h	96h	97h	98h	99h	9Ah	9Bh	9Ch	9Dh	9Eh	9Fh
Character	User-Programmable Fonts															
Index (Hex)	A0h	A1h	A2h	A3h	A4h	A5h	A6h	A7h	A8h	A9h	AAh	ABh	ACh	ADh	AEh	AFh
Character	User-Programmable Fonts															
Index (Hex)	B0h	B1h	B2h	B3h	B4h	B5h	B6h	B7h	B8h	B9h	BAh	BBh	BCh	BDh	BEh	BFh
Character	User-Programmable Fonts															
Index (Hex)	C0h	C1h	C2h	C3h	C4h	C5h	C6h	C7h	C8h							
Character	CR	2B	3B	4B	5B	6B	7B	8B	9B							

CR: Character Return / Line Feed

nB: Number of Space Characters

Another type of memory is called the “command memory”, which stores the sequence and the attribute of the font that is appearing on the screen. The command memory consists of two 256 x 8-bit RAMs in two modes (*Table 10.3.2*). In COLR mode, the command memory stores 256 font indexes with 8-bit attributes of blinking, and sixteen colors for foreground and background; and in CCAP mode, the command memory stores 256 font indexes each with 8-bits attributes of blinking, *Italic* font option, underline font option, eight colors for foreground, and four colors for background.

Table 12.3.2 Command Memory Configuration

Register CCMODE	Description	Note
0	COLR Mode	Stores 256 font indexes with attribute for color support
1	CCAP Mode	Stores 256 font indexes with attribute for closed caption support

To generate OSD in either mode, the command memory needs to be well programmed. It is divided into title, content, and bottom sections of which initial address pointed by the registers OSDT_MADR,

OSDC_MADR, and OSDB_MADR (*Figure 12.3.1*). From the initial address in each section, fill in the indexes of fonts in designated sequence, and the font will appear on the screen consecutively at the next frame. Sections allocated in the command memory can be overlaped with others.

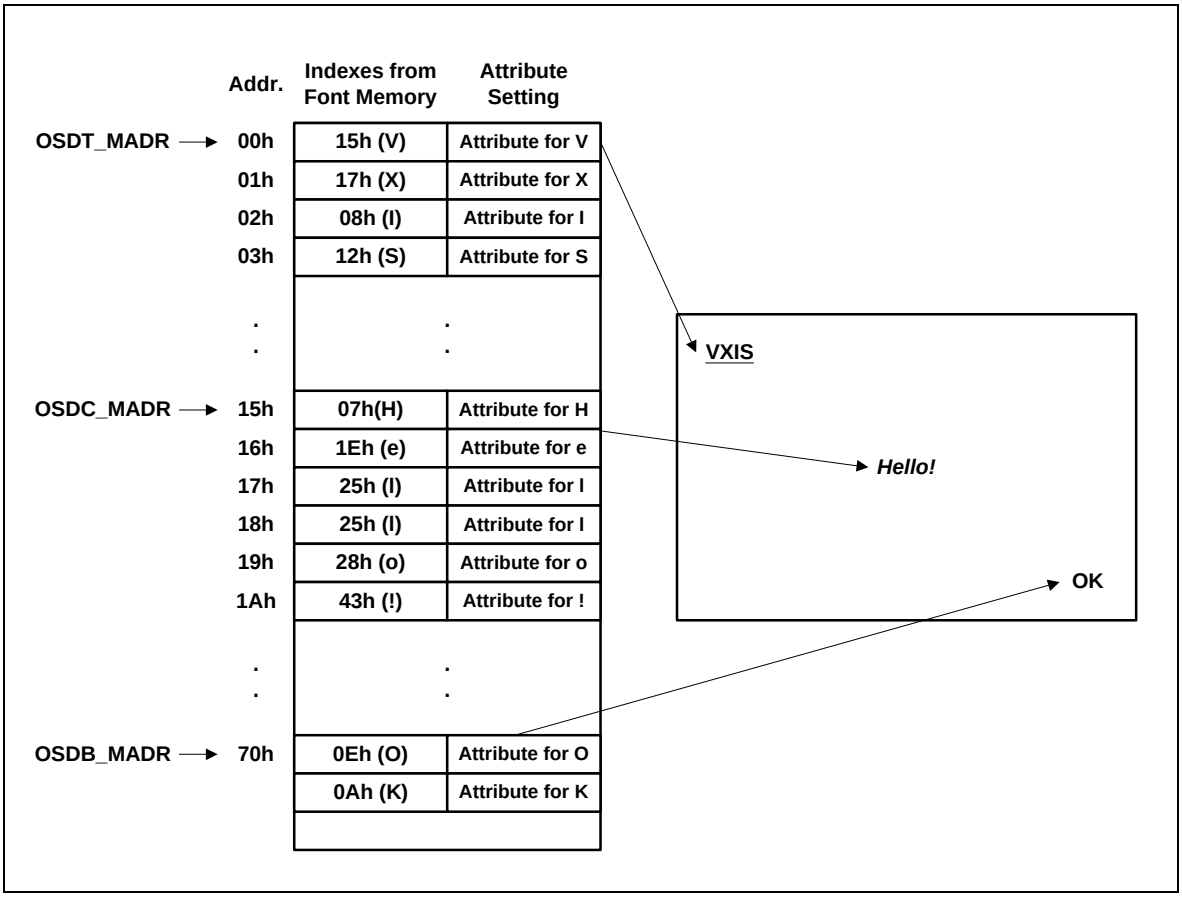


Figure 12.3.1 OSD Command Memory

12.4 OSD ATTRIBUTE SETTING

Each font displayed on the screen has its own 8-bit attributes for blinkings, colors, and special font formats. They are slightly different in CLOR mode and CCAP mode (*Table 12.4.1*).

Table 12.4.1 Attribute Bits Table

Bit	CLOR Mode	CCAP Mode
7	Blinking On	
6	BG Palette Color Index [2]	*Italic* Font On
5	BG Palette Color Index [1]	BG Color Index [1]

4	BG Palette Color Index [0]	BG Color Index [0]
3	FG Palette Color Index [3]	Underline Font On
2	FG Palette Color Index [2]	FG Palette Color Index [2]
1	FG Palette Color Index [1]	FG Palette Color Index [1]
0	FG Palette Color Index [0]	FG Palette Color Index [0]

There are sixteen blinking-rate options from 0.5 Hz to 7.5 Hz defined in the register, OSD_BLINK. The blinking-rate relates to the OSD_BLINK according to the following equation.

$$\text{OSD Blinking Rate} = \frac{30}{\text{OSD\_BLINK} \times 4}\ \text{Hz}$$

The OSD unit has sixteen build-in color palettes each can be fine adjusted from 24-bit color space (16,777,216 colors). Color palette programming can be achieved through the registers, OSD_CP_INDEX, OSD_CP_R, OSD_CP_G, and OSD_CP_B. In CLOR mode, the foreground color of each font is chosen from the color palette index 0 to 15 (FG Palette Color Index [3:0]); the background color from index 8 to 15 (BG Palette Color Index [2:0]). As in CCAP mode, the foreground color of each font is chosen from the color palette index 0 to 7 (FG Palette Color Index [2:0]); the background color of each font is chosen from the registers CCAP_BG0, CCAP_BG1, CCAP_BG2, and CCAP_BG3 with index (BG Color Index [1:0]). For CCAP_BG settings check *Table 12.4.2*.

Table 12.4.2 CCAP_BG Color Setting

CCAP_BG Bits	Color	CCAP_BG Bits	Color
0000	Black	1000	Transparent
0001	Blue	1001	Royal Blue
0010	Green	1010	Medium Aquamarine
0011	Aqua	1011	Light Green
0100	Red	1100	Orange
0101	Fuchsia	1101	Hot Pink
0110	Yellow	1110	Silver
0111	White	1111	Gray

The register, TRAN_INDEX, assigns the color palette index in which stands for transparent color.

12.5 OSD MASKING AND ALPHA-BLENDING

The VX8812's OSD unit provides special masking function in the content displaying block. This is mainly for the scrolling function during closed caption displaying. The registers, OSDC_MASK_L, OSDC_MASK_R, OSDC_MASK_T, and OSDC_MASK_B define the boundary location for the four sides of the masking blocks.

The VX8812's OSD unit also support whole screen OSD alpha-blending with the source video. The blending factor, OSD_ALPHA, is programmable in registers and follows below equation.

$$\text{OSD Displaying Color} = \frac{\text{Video Color} \times \text{OSD\_ALPHA} + \text{OSD Color} \times (4 - \text{OSD\_ALPHA})}{4}$$

12.6 OSD MEMORY ACCESS

To configure the command memory and the user-programmable font memory, the VX8812 provides two methods by accessing registers. One method is through the direct memory accessing registers OSD_ADDR, OSD_DATA, and OSD_ATRI for command memory, and registers OSD_FONT_ADDR, OSD_FONT_DATA for user-programmable font memory. The other method is through the continuous writing mechanism with Continuous-Write Registers, CW_DEST, CW_INIT_ADDR, and CW_DATA.

12.6.1 DIRECT MEMORY ACCESS

To directly change the content of the command memory, simply put the address in register OSD_ADDR and the data in registers OSD_DATA and OSD_ATRI. The OSD unit will send the data into the command memory right after the register writing operation of register OSD_DATA and OSD_ATRI. Similarily, to directly change the content of the user-programmable font memory, user simply puts the address in the register OSD_FONT_ADDR and the data in the register OSD_FONT_DATA from high byte to low byte. The OSD unit will send the data into the user-programmable font memory right after the writing operation of low byte of OSD_FONT_DATA.

12.6.2 CONTINUOUS WRITE MEMORY ACCESS

For large amount of data writing operation such as font memory writing or full screen display change, the VX8812 provides continuous writing mechanism to save host access time and efforts. To use the Continuous-Write Registers, set the destination register, CW_DEST, and the initial address register,

CW_INIT_ADDR, consecutively, then write the data register, CW_DATA, repeatly. The continuous-writing mechanism will put data into the destination memory immediately after CW_DATA writing. For 16-bit data writing such as user-programmalbe font memory, the internal memory data writing will occur after every other CW_DATA writing (high byte prior to low byte). For example, to store a plus sign, "+", into the user-programmalbe font memory, the writing sequence are as *Table 12.6.2.1*.

Table 12.6.2.1 Host Writing Sequence for Bitmap

Host Command	Address	Data
Write	CW_DEST	010
Write	CW_INIT_ADDR	00_0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0011_1111
Write	CW_DATA	1111_1100
Write	CW_DATA	0011_1111
Write	CW_DATA	1111_1100
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000

Host Command	Address	Data
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000

13 ELECTRICAL CHARACTERISTICS

13.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage For Digital Core (1.8V Nominal)	V_{CCC}	-0.3	1.98	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	-0.3	3.6	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	-0.3	3.6	V
Junction Temperature	T_J	-40	125	°C
Storage Temperature	T_{STG}	-55	125	°C
Lead Temperature (Vapor Phase Soldering, 40 Seconds)	T_L	-	215	°C
Electronic Discharge	T_{ESD}	-2000	2000	V

13.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage For Digital Core (1.8V Nominal)	V_{CCC}	1.62	1.8	1.98	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	3.0	3.3	3.6	V
Supply Voltage For Analog Core (1.8V Nominal)	V_{DDA}	1.62	1.8	1.98	V
Ambient Operation Temperature	T_A	0	-	70	°C
Package Case Temperature	T_A	-	-	115	°C
Total Power Dissipation	P_{TOT}	-	TBA	-	W

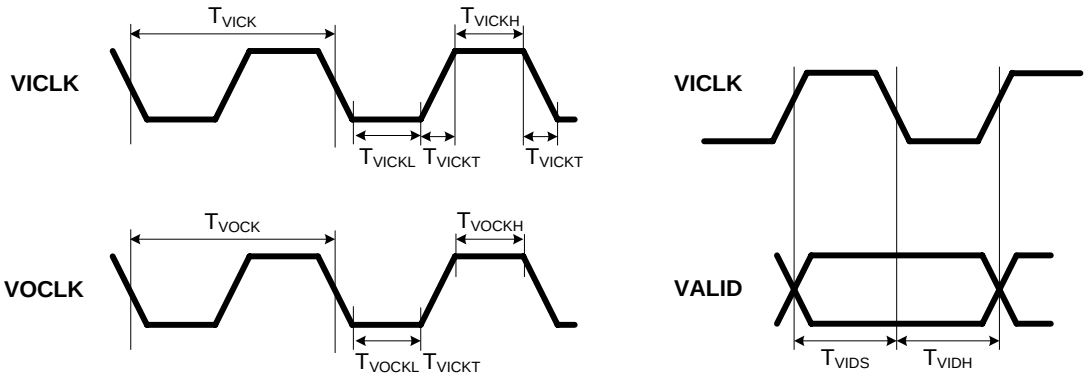
13.3 DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input (I, I_S, I_{PU}, I_{PD})					
High Level Input Voltage	V_{IH}	2	-	3.6	V
Low Level Input Voltage	V_{IL}	-0.3	-	0.8	V
Leakage Current	I_L	-15	-	+10	nA
Output (O_1, O_{TS1})					
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Tri-State Output Leakage Current	I_L	-15	-	+10	nA
Pull-Up/Down Resistor					
Pull-Up Resistor	R_{PU}	-	50	-	KΩ
Pull-Down Resistor	R_{PD}	-	50	-	KΩ

13.4 AC CHARACTERISTICS

13.4.1 VIDEO INTERFACE

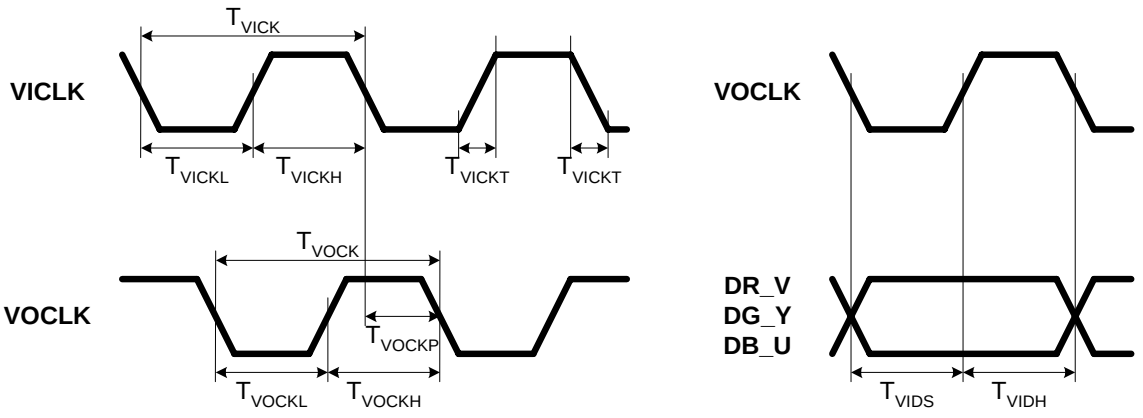
Parameter	Symbol	Min	Typ	Max	Unit
Digital Video Clocks					
Video Input Clock VICLK Frequency	F_{VICK}	-	27	150	MHz
Video Input Clock VICLK Transition Time	T_{VICKT}	-	0.5	-	ns
Video Output Clock VOCLK Frequency	F_{VOCK}	-	27	27	MHz
					ns
Digital Video Input					
Video Input Data Setup Time To VICLK	T_{VIDS}	-	-3.0	-	ns
Video Input Data Hold Time From VICLK	T_{VIDH}	-	1.78	-	ns
Digital Video Output					
Video Output Data Delay From VOCLK	T_{VODH}	-	1	-	ns



Digital Video Interface Timing

13.4.2 HOST INTERFACE

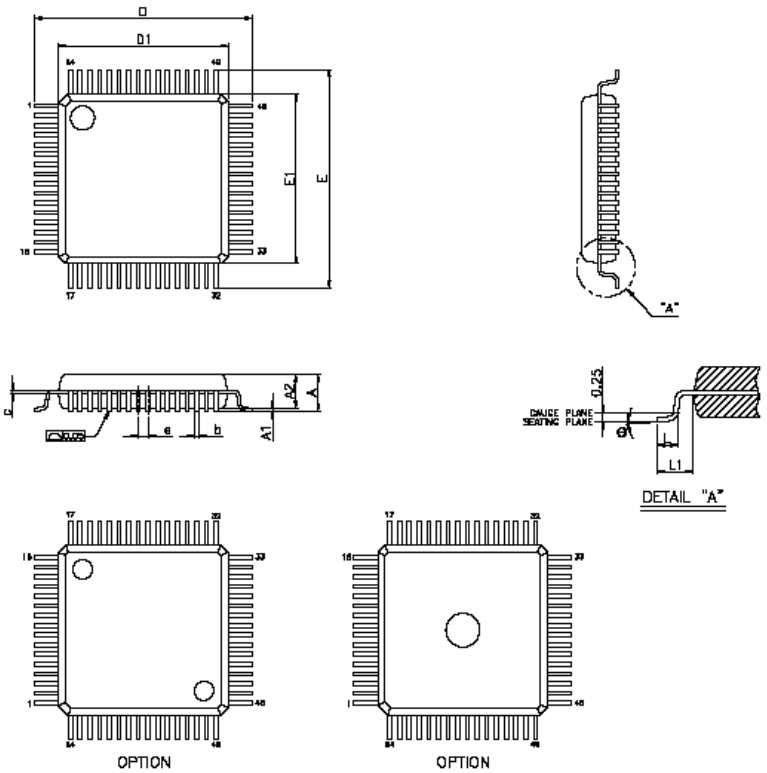
Parameter	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency	F_{SCL}	-	100	-	KHz
Serial Bus Free Time Between STOP and START Condition	T_{BUF}	4.7	-	-	µs
Serial Bus Hold Time For START Condition	T_{HDSTA}	4.0	-	-	µs
SCL Clock Width Low	T_{SCLL}	4.7	-	-	µs
SCL Clock Width High	T_{SCLH}	4.0	-	-	µs
Serial Data Setup Time	T_{HSDS}	0.5	-	-	µs
Serial Data Hold Time	T_{HSDH}	-	-	0	µs
Serial Bus Setup Time For STOP Condition	T_{SUSTO}	4.0	-	-	µs



Digital Video Interface Timing

14 PACKAGE

14.1 VX8812 64PIN-LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.