VS9126

TRIPLE 10-BIT HIGH SPEED

VIDEO DAC

AND

MULTI-FORMAT

SD/HD VIDEO ENCODER

Headquarters Room B7, 1F, No.1, Li_Hsin Rd. I, Science Based Industrial Park, HsinChu City, 300, Taiwan, R.O.C. Tel : 886-3-5630888 Fax: 886-3-5630889		VXIS Technology Corp. http://www.vxis.com

Table of Contents

1 OVERVIEW

1.1 DESCRIPTION

The VS9126 is a triple high speed digital to analog converter and a high definition video encoder IC for different video format output. It supports composite CVBS / S-video output, and component YPbPr / RGB output.

The VS9126 has 30-bit digital input, It can support three 10-bit/8-bit RGB inputs or YUV inputs with hsync and vsync, also it can support 16-bit BT.1120 with embedded sync or 10-bit/8-bit BT.601 input with external sync, or BT.656 with embedded sync. The maximum supported input frequency is 160MHz data rate.

The VS9126 has three 10-bit 200MHz DAC output which can reach the higher quality and resolution for analog video output application. The maximum supported resolution including HDTV 1080P@60, VESA 1920x1200@60.

The VS9126 can encode the 480i or 576i digital input to CVBS or S-video output, also it can encode 480P or 576P digital input to CVBS or S-video output. Any other digital input data can be transferred to its corresponding analog output format, such as 1080P digital RGB/YUV input can be transferred to 1080P analog RGB or YPbPr output.

There is a hardware auto resolution detected mode to transfer the input data correctly to its corresponding output format, just by configuring the corresponding input mode and output mode setting pin, no external micro-controller needed. If necessary, there are also 2-wire serial control i2c pin to control the internal processing registers, such as brightness, contrast, saturation and hue adjustment or input data horizontal and vertical shift.

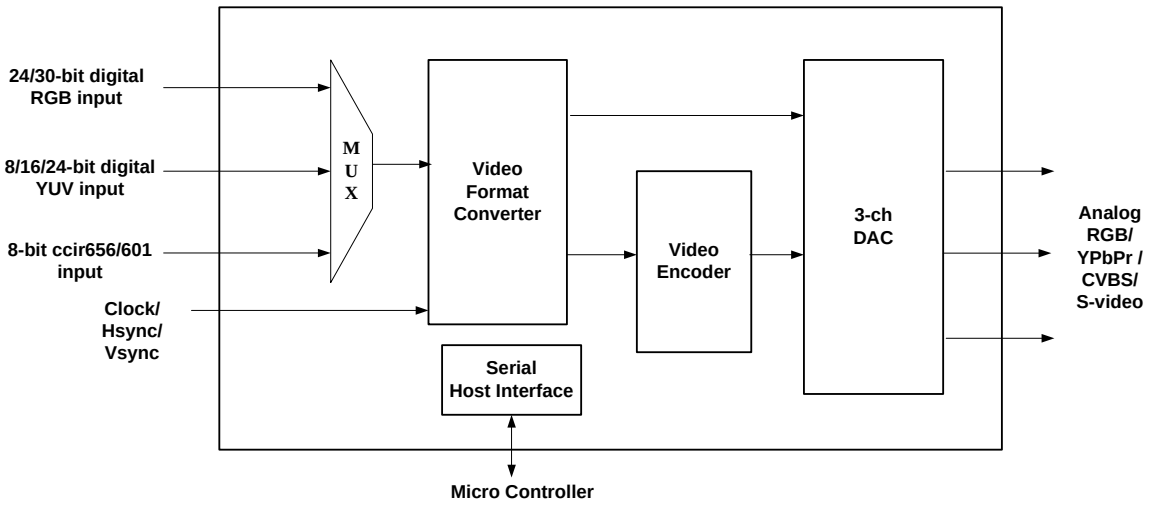
1.2 APPLICATION

- Surveillance
- Set-top box
- Video converter
- Multimedia panel

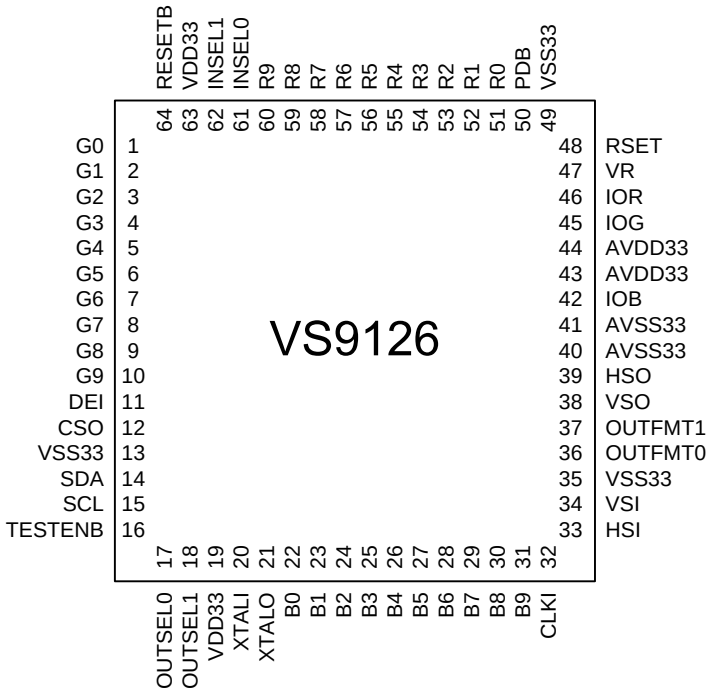
1.3 FEATURES

- Support Various digital video Input
  - RGB 24/30 bit
  - YUV 24/30 bit
  - YUV 16/20 bit (or BT1120)
  - YUV 8/10 bit (BT656,BT601)
  - Max data rate 160MHz
- Support Various Analog Output Formats
  - Composite video output (NTSC/PAL)
  - S-video output (NTSC/PAL)
  - Analog R/G/B output + Horizontal Sync + Vertical Sync
  - Analog Y/Pb/Pr output
  - Max output resolution 1080P@60
- 480P to NTSC, 576P to PAL convert
- Active data shift in horizontal and vertical direction
- Horizontal and vertical sync pulse size adjustment
- Data mask
- Video Brightness,contrast,saturation,hue adjustment
- R/G/B input port swap & rotation control
- Input resolution auto detect
- 2 wire serial control
- 3.3V tolerant I/O
- 3.3V power supply only
- 64 pin

1.4 BLOCK DIAGRAM



1.5 PINOUT DIAGRAM



1.6 PIN ASSIGNMENT

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	G0	17	OUTSEL0	33	HSI	49	VSS33
2	G1	18	OUTSEL1	34	VSI	50	PDB
3	G2	19	VDD33	35	VSS33	51	R0
4	G3	20	XTALI	36	OUTFMT0	52	R1
5	G4	21	XTALO	37	OUTFMT1	53	R2
6	G5	22	B0	38	VSO	54	R3
7	G6	23	B1	39	HSO	55	R4
8	G7	24	B2	40	VSS33	56	R5
9	G8	25	B3	41	VSS33	57	R6
10	G9	26	B4	42	IOB	58	R7
11	DEI	27	B5	43	VDD33	59	R8
12	CSO	28	B6	44	VDD33	60	R9
13	VSS33	29	B7	45	IOG	61	INSEL0
14	SDA	30	B8	46	IOR	62	INSEL1
15	SCL	31	B9	47	VR	63	VDD33
16	TESTENB	32	CLKI	48	RSET	64	RESETB

1.7 PIN DESCRIPTION

Video Input Pins

Name	Type	Description	Notes
R9~R0	I	Digital Video Input R/Cr Data	
G9~G0	I	Digital Video Input G/Y Data	
B9~B0	I	Digital Video Input B/Cb Data	
CLKI	I	Digital Video Input Clock	
HSI	I	Digital video input horizontal synchronization	
VSI	I	Digital video input vertical synchronization	
DEI	I	Digital Video data enable input	

Video Output Pins

Name	Type	Description	Notes
IOR	O	R/Pr/S-Y Analog Video Output	
IOG	O	G/Y /CVBS Analog Video Output	
IOB	O	B/Pb/S-C Analog Video Output	
HSO	O	video output horizontal synchronization	
VSO	O	video output vertical synchronization	
CSO	O	composite sync output	

Miscellaneous I/O Pins

Name	Type	Description	Notes
/RESETB	I_{PU}	Chip Reset (Active Low)	
XTAL_OUT	XO	Crystal Output	
XTAL_IN	XI	Crystal Input	
SDA	I_{PU}/O	Host Interface Serial Data / Address	
SCL	I_{PU}	Host Interface Serial Clock	
/TESTENB	I_{PU}	Test Mode Enable (Active Low)	
INSEL1, INSEL0	I	Input mode select	
OUTSEL1, OUTSEL0	I	Output mode select	
OUTFMT1, OUTFMT0	I	CVBS output format select	
PDB	I	power down pin, low to power down.	
RSET	A	resistor connection for DAC gain adjustment	
VR	A	voltage reference for DAC, connect to Cap.	

Power Pins

Name	Type	Description	Notes
VDD33	P_{33}	Digital 3.3V power for I/O	Qty: 2

VSS33	G	Digital Ground For I/O	Qty: 3
AVDD33	P_{33}	Analog 3.3V power for DAC	Qty: 2
AVSS33	G	Analog ground for DAC	Qty: 2

note :

I	3.3V input
O	3.3V output
I/O	3.3V input/output
I_{PU}	3.3V input with internal pull up
XI,XO	crystal input, output pin
P_{33}	3.3V power pin
P_{18}	1.8V power pin
G	Ground pin

1.8 PACKAGE

- 9126 64-Pin LQFP

2 VIDEO I/O PIN ASSIGNMENT

2.1 DIGITAL VIDEO INPUT ASSIGNMENT

The VS9126 digital video interface is compatible with extensive digital video output standard formats. As for inputs, VS9126 directly supports 8-bit YUV with (ITU-R BT.656) or without (ITU-R BT.601) embedded synchronization, it also supports 16-bit Y/UV, 24-bit YUV, 24-bit RGB input and BT.1120 format. In the hardware mode(register IIC_MODE=0), the input format is decided by the pin {INSEL1,INSEL0}. In the IIC_MODE(register IIC_MODE=1), the input format is decided by the regitsers INFMT[1:0].

The pin arrangement for each input format is defined in *Table 2.1.*

Pin Name	I/O Type	INSEL[1:0]							
		0		1		2		3	
		30-bit RGB	24-bit RGB	30-bit YUV	24-bit YUV	20-bit YUV	16-bit YUV	10-bit YUV	8-bit YUV
R9	I	R[9]	R[7]	V[9]	V[7]	-	-	-	-
R8	I	R[8]	R[6]	V[8]	V[6]	-	-	-	-
R7	I	R[7]	R[5]	V[7]	V[5]	-	-	-	-
R6	I	R[6]	R[4]	V[6]	V[4]	-	-	-	-
R5	I	R[5]	R[3]	V[5]	Y[3]	-	-	-	-
R4	I	R[4]	R[2]	V[4]	V[2]	-	-	-	-
R3	I	R[3]	R[1]	Y[3]	V[1]	-	-	-	-
R2	I	R[2]	R[0]	V[2]	V[0]	-	-	-	-
R1	I	R[1]	-	V[1]	-	-	-	-	-
R0	I	R[0]	-	V[0]	-	-	-	-	-
G9	I	G[9]	G[7]	Y[9]	Y[7]	Y[9]	Y[7]	YUV[9]	YUV[7]
G8	I	G[8]	G[6]	Y[8]	Y[6]	Y[8]	Y[6]	YUV[8]	YUV[6]
G7	I	G[7]	G[5]	Y[7]	Y[5]	Y[7]	Y[5]	YUV[7]	YUV[5]
G6	I	G[6]	G[4]	Y[6]	Y[4]	Y[6]	Y[4]	YUV[6]	YUV[4]
G5	I	G[5]	G[3]	Y[5]	Y[3]	Y[5]	Y[3]	YUV[5]	YUV[3]
G4	I	G[4]	G[2]	Y[4]	Y[2]	Y[4]	Y[2]	YUV[4]	YUV[2]
G3	I	G[3]	G[1]	Y[3]	Y[1]	Y[3]	Y[1]	YUV[3]	YUV[1]
G2	I	G[2]	G[0]	Y[2]	Y[0]	Y[2]	Y[0]	YUV[2]	YUV[0]
G1	I	G[1]	-	Y[1]	-	Y[1]	-	YUV[1]	-
G0	I	G[0]	-	Y[0]	-	Y[0]	-	YUV[0]	-
B9	I	B[9]	B[7]	U[9]	U[7]	UV[9]	UV[7]	-	-
B8	I	B[8]	B[6]	U[8]	U[6]	UV[8]	UV[6]	-	-
B7	I	B[7]	B[5]	U[7]	U[5]	UV[7]	UV[5]	-	-
B6	I	B[6]	B[4]	U[6]	U[4]	UV[6]	UV[4]	-	-
B5	I	B[5]	B[3]	U[5]	U[3]	UV[5]	UV[3]	-	-
B4	I	B[4]	B[2]	U[4]	U[2]	UV[4]	UV[2]	-	-
B3	I	B[3]	B[1]	U[3]	U[1]	UV[3]	UV[1]	-	-
B2	I	B[2]	B[0]	U[2]	U[0]	UV[2]	UV[0]	-	-
B1	I	B[1]	-	U[1]	-	UV[1]	-	-	-
B0	I	B[0]	-	U[0]	-	UV[0]	-	-	-

2.2 ANALOG VIDEO OUTPUT ASSIGNMENT

The VS9126 can send different analog output video of format RGB, YpbPr, CVBS or S-video. In the hardware mode(register IIC_MODE=0), the output format is decided by the pin {OUTSEL1,OUTSEL0}. In the IIC_MODE(register IIC_MODE=1), the output format is decided by the register OUTFMT[1:0].

The pin assignment for each format is defined in *Table 2.2*

Table 2.2 Analog Video Output Pin Assignment

Pin Name	I/O Type	OUTSEL[1:0]			
		0	1	2	3
IOR	**O**	R	Pr	S-Y	CVBS
IOG	**O**	G	Y	CVBS	CVBS
IOB	**O**	B	Pb	S-C	CVBS

2.3 CVBS OUTPUT STANDARD ASSIGNMENT

If the video output is assigned to CVBS, then the CVBS output standard is set by the pins {OUTFMT1,OUTFMT0} in the hardware mode(register IIC_MODE=0). And it also can be set by the registers TVSTD[1:0] in the IIC_MODE(register IIC_MODE=0) .

The VS9126 will auto detect the input VSYNC frequency. If the frequency is 60Hz, then the CVBS output format will be selected in the 60 field/s group. If the frequency is 50Hz, then the CVBS output format will be selected in the 50 field/s group according to the OUTFMT pin setting.

The pin assignment for each format is defined in *Table 2.3*

Table 2.3 Analog Video Output Pin Assignment

OUTFMT	60 field/s	50 field/s
00	NTSC-M	PAL-B,G,D,I
01	NTSC-J	PAL-N
10	PAL-M	PAL-Nc
11	-	-

3 CLOCK AND DATA

There are two reference clocks for VS9126. The CLKI is the input data sampling clock, the crystal is used for internal registers processing. If there are no registers setting required, the crystal can be saved, and tie the crystal pin to ground.

In general, the input digital data are sampled at the rising edge of CLKI, as in figure 3.1. If the input data transition is aligned with the clock rising edge, then register VICLKP should be set to 1, to inverse the input clock, so data is sampled at the falling edge of the CLKI.

For the convenience of board design, the input RGB data can be swap to BGR or RBG or … , by setting the register RGB_MUX. Also, the bit order of each RGB data can be swap by setting the register R_INV, G_INV, B_INV.

4 HOST INTERFACE

The VS9126 host interface uses two-wire IIC compatible interface protocol, one for clock, and one for multiplexed data/address. Input pin SCL is used for host clock input while input/output pin SDA is for multiplexed host data and address signal. The chip read address is 0x26, and write address is 0x27. Once chip write and read addresses are configured, the host command byte sequence can be transfer to VS9126 via the serial interface. The byte sequence consists of a CHIP ADDRESS, a REGISTER ADDRESS, followed by a number of DATA BYTES. The CHIP ADDRESS and REGISTER ADDRESS must be always provided by the host, usually a micro-controller, and the DATA BYTES are provides by host for host-writings and by VS9126 for host-readings.

Fig 3.1 Host command write sequence

Fig 3.2 Host command read sequence

As shown above, the first DATA BYTE following REGISTER ADDRESS A is assigned or read to/from register address A, the DATA BYTE behind will be assigned/read to/from register address A+1, and so on. So for large host-writings such as chip initialization, only the initial register address needs to be specified once to complete whole host writing operations. In this manner user can save a lot of host command cycles in complicated applications.

5 HARDWARE AND SOFTWARE RESET

VS9126 can be reset to initial status in two ways. One is through the hardware pin, RESETB; by asserting RESETB pin to ground, entire chip will be reset to its initial states. The other way is through the host interface by writing to register RST1 (0x01). Writing value 0x5A to RST1, called software reset, will generate an internal reset pulse signal similar to RESETB to initialize the entire chip.

Similar to writing 0x5A to RST1, writing 0xA5 to RST1 will reset entire chip *except* control registers programmed by host interface. The use of 0xA5 writing often occurs after initial register programming or mid-state register changes to assure the chip working from the initial state.

6 COLOR ENHANCEMENT

6.1 CONTRAST, BRIGHTNESS, COLOR, AND HUE ADJUSTMENT

The VS9126 supports essential color adjustment through the registers, CONTRAST, BRIGHTNESS, COLOR, and HUE. Among those, the CONTRAST and the BRIGHTNESS can also be adjusted independently in R / G / B manner by the registers, R_CONTRAST, G_CONTRAST, B_CONTRAST, R_BRIGHTNESS, G_BRIGHTNESS, and B_BRIGHTNESS.

7 VIDEO OUTPUT DISPLAY

7.1 CLAMPING

The VS9126 has an option to set the digital video output level in ITU-R BT.601 range, ITU-R BT.656 range, or simply in 0-255 8-bit full range by setting the register CLAMP value. . For ITU-R BT.601 standard, luminance channel (Y) is in the range of 16-235, and chrominance channel (UV) is in the range of 16-240, CLAMP is set to 1. For ITU-R BT.656 standard, luminance (Y) and chrominance channel (UV) are in the range of 1-254, CLAMP is set to 2. Otherwise, CLAMP is set to 0, without changing the output level.

7.2 VIDEO OUTPUT DISPLAY

Two essential elements, screen shifting and masking, control the VS9126 video output display. The screen shifting function is activated by changing the horizontal shifting register HSHIFT, and vertical shifting register VSHIFT. Setting the MSB value of HSHIFT (HSHIFT[11]) to 1 moves the picture leftward, and setting the MSB value to 0 moves the picture rightward. Also, setting the MSB value of VSHIFT (VSHIFT[11]) to 1 moves the picture upward, and setting the MSB value to 0 moves the picture downward.

The screen masking function is activated by setting the registers MASK_EN=1 to enable data masking. The registers BOTTOM_MASK, TOP_MASK, LEFT_MASK, RIGHT_MASK are used to set the four boundary of data masking.

The input horizontal total length, and active data length are auto-detected and can be read from registers HIN_TOTAL, HIN_ACT. The input vertical total line number, and active data line number are auto-detected and can be read from registers VIN_TOTAL, VIN_ACT.

The VS9126's output display region with its synchronization and control parameters (screen shifting and screen masking) is described in *Figure 7.2.1*.

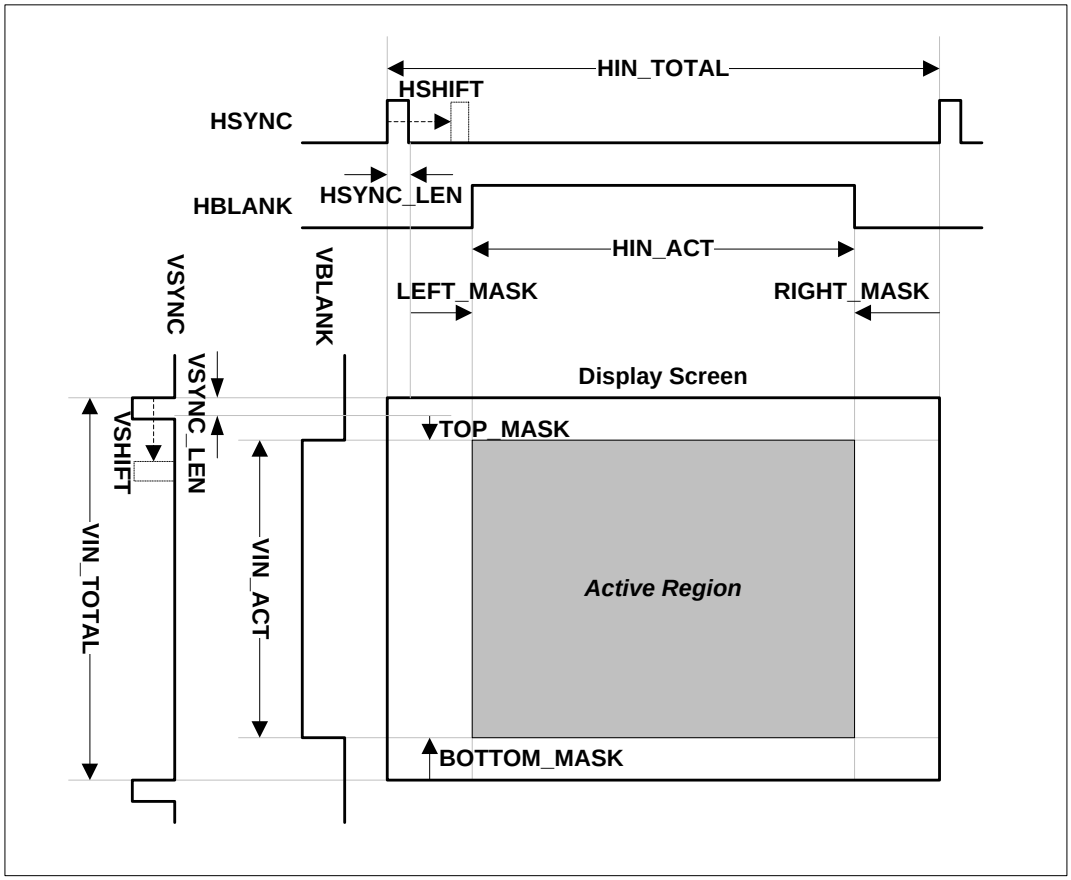


Figure 7.2.1 Output Display Region

8 REGISTER DESCRIPTION

8.1 PROGRESSIVE VIDEO PROCESSOR REGISTER

8.1.1 REGISTER MAP (CHIP ADDRESS = 0X26)

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01	IN1	00	RESET / CLEAR							
02	IN2	10	CLKD2	VIHSP	VIVSP	EXTSYNC	CBIT10	INPMUL	INFMT	
03	IN3	00	HS_SEL	IIC_MODE	VOHSP	VOVSP	TVSTD		OUTFMT	
04	IN4	41	NPALX2	CLAMP		P2I	YPBPR_FMT	YPBPR_INT	SD_NPAL	FBPOR_EN
05	IN5	7e	YPBPR_SYNC							
06	IN6	00	SYNC_DIS	FSO_EN	R_INV	G_INV	B_INV	RGB_MUX		
07	IN7	08	DDRIN_EN	CSYNCIN_EN	VIDEP	DE2HS	-	-	-	-
08	IN8	01	-	VIFSP	VOCS_SEL			DE_MASK_EN	VICLK_DLY	
10(R)	DE0	00	HIN_TOTAL[11:8]				HIN_ACT[11:8]			
11(R)	DE1	00	HIN_TOTAL[7:0]							
12(R)	DE2	00	HIN_ACT[7:0]							
13(R)	DE3	00	VIN_TOTAL[11:8]				VIN_ACT[11:8]			
14(R)	DE4	00	VIN_TOTAL[7:0]							
15(R)	DE5	00	VIN_ACT[7:0]							
16(R)	DE6	00	NPALX2_DET	HD_SD_DET	SD_NPAL_DET	INTERLACE_DET	480P_DET	VSPOL_DET	HSPOL_DET	SYNC_DET
20	OS0	88	VSHIFT[11:8]				HSHIFT[11:8]			
21	OS1	00	VSHIFT[7:0]							
22	OS2	00	HSHIFT[7:0]							
23	OS3	00	-		VSYNC_LEN[9:8]		-		HSYNC_LEN[9:8]	
24	OS4	08	VSYNC_LEN[7:0]							
25	OS5	40	HSYNC_LEN[7:0]							
26	OS6	02	-	-	-	-	-	-	SYNC_MASK_EN	MASK_EN
27	OS7	00	LEFT_MASK[11:8]				RIGHT_MASK[11:8]			
28	OS8	00	LEFT_MASK[7:0]							
29	OS9	00	RIGHT_MASK[7:0]							
2A	OSA	00	TOP_MASK[11:8]				BOTTOM_MASK[11:8]			
2B	OSB	00	TOP_MASK[7:0]							
2C	OSC	00	BOTTOM_MASK[7:0]							
30	DA0	18	-	-	DAC_CLK_INV	RGB_BYPASS	BLANKB	SYNCB	DAC_CKPOL	PD_DAC
31	DA1	dc	CVBS_BLANK_VAL							
32	DA2	20	CVBS_N_SAV							
33	DA3	20	CVBS_N_EAV							
34	DA4	34	CVBS_P_SAV							
35	DA5	18	CVBS_P_EAV							
38	GC0	00	GCSYNC_EN	-	-	FIELD_IN	GC_INV	GC_XOR	VIN_P	HIN_P
39	GC1	00	H_FALL[11:8]				H_RISE[11:8]			
3A	GC2	00	H_RISE[7:0]							
3B	GC3	00	H_FALL[7:0]							
3C	GC4	00	V_FALL[11:8]				V_RISE[11:8]			

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
3D	GC5	00	V_RISE[7:0]							
3E	GC6	00	V_FALL[7:0]							
40	PA0	80	BRIGHTNESS							
41	PA1	80	CONTRAST							
42	PA2	80	SATURATION							
43	PA3	20	-	-	HUE					
44	PA4	80	R_BRI							
45	PA5	80	G_BRI							
46	PA6	80	B_BRI							
47	PA7	80	R_CON							
48	PA8	80	G_CON							
49	PA9	80	B_CON							
50	PT0	30	PAT_EN	GEN_SYNC	PT_VPOL	PT_HPOL	PAT_MODE			
51	PT1	43	PT_HLEN[11:8]				PT_HACT[11:8]			
52	PT2	1F	PT_HLEN[7:0]							
53	PT3	1F	PT_HACT[7:0]							
54	PT4	22	PT_VLEN[11:8]				PT_VACT[11:8]			
55	PT5	73	PT_VLEN[7:0]							
56	PT6	53	PT_VACT[7:0]							
57	PT7	00	PT_YVAL[7:0]							
58	PT8	81	PT_YVAL[9:8]		PT_INCVAL					
59	PT9	01	PT_INTLEN							
5A	PTA	0a	-	-	-	D656_EN	PT_CBVAL[9:8]		PT_CRVAL[9:8]	
5B	PTB	00	PT_CBVAL[7:0]							
5C	PTC	00	PT_CRVAL[7:0]							

8.1.2 REGISTER DESCRIPTION

8.1.2.1 GLOBAL REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01	IN1	-	RESET / CLEAR							

RESET Software reset all circuits by writing 5Ah

CLEAR Software reset all circuits other than registers by writing A5h

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
02	IN2	10	VICLKP	VIHSP	VIVSP	EXTSYNC	CBIT10	INPMUL	INFMT	

VICLKP

0 Normal (df.)

1 Inverse VICLK pin polarity

VIHSP

0 Normal (df.)

1 Inverse the hsync input pin HSI polarity

VIVSP

0 Normal (df.)

1 Inverse the vsync input pin VSI polarity

EXTSYNC

valid only when IIC_MODE=1

0 Normal

1 Use HIS,VIS pin as sync input (df.)

CBIT10

0 Treat input data bus as 8 bit (df.)

1 Treat input data bus as 10 bit

INPMUL

0 Input sync polarity is controlled automatically (df.)

1 input sync polarity is controlled by register VIHSP,VIVSP

INFMT[1:0]

Set the input data format, valid only when IIC_MODE=1

00 Input data are RGB 24/30 bits (df.)

01 Input data are YUV 24/30 bits

10 Input data are YUV 16/20 bits

11 Input data are YUV 8/10 bits

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
03	IN3	00	HS_SEL	IIC_MODE	VOHSP	VOVSP	TVSTD		OUTFMT	

These registers are valid only when IIC_MODE=1

HS_SEL

0 Output hsync to Pin HSO (df.)

1 Output composite sync to pin HSO

IIC_MODE

0 hardware auto detected mode (df.)

1 Enable internal registers controlled by I2C

VOHSP

0 Normal (df.)

1 Inverse the hsync output pin HSO polarity

VOVSP

0 Normal (df.)

1 Inverse the vsync output pin VSO polarity

TVSTD[1:0]

The CVBS output standard select, valid only when IIC_MODE=1

frame rate	60	50
00	NTSC-M	PAL-B,G,D,I
01	NTSC-J	PAL-N
10	PAL-M	PAL-Nc
11	-	-

OUTFMT[1:0]

The analog video output format select,

valid only when IIC_MODE=1

00 Output signals are analog RGB (df.)

01 Output signals are analog YPbPr

10 Output signals are CVBS + S-Video

11 Output signals are all CVBS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
04	IN4	41	CLKD2	CLAMP		P2I	YPBPR_FMT	YPBPR_INT	SD_NPAL	-

These registers are valid only when IIC_MODE=1

CLKD2 Set the input clock sampling rate

0 normal (df.)

1 1/2 sampling down clock rate

CLAMP[1:0] Video output data clamping control

00 Video output is in the range of 0 – 255.

01 Video output is in the range of 16 – 235 (Y), 16 –240 (UV)

10 Video output is in the range of 1 – 254. (df.)

11 Reserved

P2I

0 Normal (df.)

1 The input data is 480P/576P and the output is CVBS

YPBPR_FMT Output YPbPr format

0 SD format (df.)

1 HD format

YPbPr_INT Output YPbPr format

0 progressive format (df.)

1 interlace format

SD_NPAL Output YPbPr format

0 60 frame output (df.)

1 50 frame output

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
05	GBL3	7e	YPBPR_SYNC							

YPBPR_SYNC[7:0] The depth of Y synchronization in YPbPr output mode

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
06	IN6	00	-	FSO_EN	R_INV	G_INV	B_INV	RGB_MUX		

FSO_EN

0 Normal (df.)

1 Enable pin G1,G0 as field and blank output

R_INV

0 Normal (df.)

1 Inverse the input data R9~R0 order to R0~R9

G_INV

0 Normal (df.)

1 Inverse the input data G9~G0 order to G0~G9

B_INV

0 Normal (df.)

1 Inverse the input data B9~B0 order to B0~B9

RGB_MUX[2:0] Swap the R,G,B input data bus.

RGBIN_MUX	R	G	B
0	R	G	B
1	R	B	G
2	G	R	B
3	G	B	R
4	B	R	G
5	B	G	R
6	R	R	R
7	G	G	G

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
07	IN7	08	DDRIN_EN	CSYNCIN_EN	VIDEP	DE2HS	-	-	-	-

DDRIN_EN

0 Latch the input data at the rising edge of input clock (df.)

1 Latch the input data at both the rising and falling edge of input clock

CSYNCIN_EN

0 No composite sync (df.)

1 Enable the composite sync procseeing

VIDEP

0 Normal (df.)

1 Inverse the input DEI pin polarity

DE2HS

0 Normal (df.)

1 Use pin HSI as DE signal input

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
08	IN8	01	-	VIFSP	VOCS_SEL			DE_MASK_EN	VICLK_DLY	

VIFSP

0 Normal (df.)

1 Inverse the input field polarity

VOCS_SEL[2:0]

Select the signal output to pin CSO

000 HSO & VSO (df.)

001 gcsync

010 blank

011 field

100 dac clock

101 HSO

110 0

111 1

DE_MASK_EN

0 Normal (df.)

1 Enable masking data according DEI

VICLK_DLY[1:0] Set delay to input clock to latch data

8.1.2.2 INPUT STATUS REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
10(R)	DE0	00	HIN_TOTAL[11:8]				HIN_ACT[11:8]			
11(R)	DE1	00	HIN_TOTAL[7:0]							
12(R)	DE2	00	HIN_ACT[7:0]							

HIN_TOTAL[11:0] Input video horizontal line length (read only)

HIN_ACT[11:0] Input video horizontal line active data length (read only)

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
13(R)	DE3	00	VIN_TOTAL[11:8]				VIN_ACT[11:8]			
14(R)	DE4	00	VIN_TOTAL[7:0]							
15(R)	DE5	00	VIN_ACT[7:0]							

VIN_TOTAL[11:0] Input video total line number per frame (read only)

VIN_ACT[11:0] Input video active data line number per frame (read only)

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
16(R)	DE6	00	-	HD_SD_DET	SD_NPAL_DET	INTERLACE_DET	480P_DET	VSPOL_DET	HSPOL_DET	SYNC_DET

HD_SD_DET The auto detected HD or SD value (read only)

0 Input resolution is SD

1 Input resolution is HD

SD_NPAL_DET The auto detected SD_NPAL value (read only)

0 Input video is 60 frame

1 Input video is 50 frame

INTERLACE_DET The auto detected INTERLACE value (read only)

0 progressive

1 interlace

480P_DET The auto detected 480P value (read only)

0 non-480P/576P input

1 480P/576P input

VSPOL_DET The auto detected VS_POL value (read only)

0 Negative vsync is detected

1 Positive vsync is detected

HSPOL_DET The auto detected HS_POL value (read only)

0 Negative hsync is detected

1 Positive hsync is detected

SYNC_DET The auto detected SYNC value (read only)

0 No external sync is detected

1 External sync is detected

8.1.2.3 OUTPUT FORMAT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
20	OS0	88	VSHIFT[11:8]				HSHIFT[11:8]			
21	OS1	00	VSHIFT[7:0]							
22	OS2	00	HSHIFT[7:0]							

VSHIFT[11:0] Shift the video in vertical direction

HSHIFT[11:0] Shift the video in horizontal direction

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
23	OS3	00	-		VSYNC_LEN[9:8]		-		HSYNC_LEN[9:8]	
24	OS4	08	VSYNC_LEN[7:0]							
25	OS5	40	HSYNC_LEN[7:0]							

VSYNC_LEN[9:0] Set the output vsync pulse length

HSYNC_LEN[9:0] Set the output hsync pulse length

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
26	OS6	02	-	-	-	-	-	-	SYNC_MASK_EN	MASK_EN

SYNC_MASK_EN Enable data mask in the sync pulse period

MASK_EN Enable data mask according the mask register setting

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
27	OS7	00	LEFT_MASK[11:8]				RIGHT_MASK[11:8]			
28	OS8	00	LEFT_MASK[7:0]							
29	OS9	00	RIGHT_MASK[7:0]							

LEFT_MASK[11:0] Number of pixels masked from the left-hand-side of a frame

RIGHT_MASK[11:0] Number of pixels masked from the right-hand-side of a frame

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
2A	OSA	00	TOP_MASK[11:8]				BOTTOM_MASK[11:8]			
2B	OSB	00	TOP_MASK[7:0]							
2C	OSC	00	BOTTOM_MASK[7:0]							

TOP_MASK[11:0] Number of lines masked from the top of a frame

BOTTOM_MASK[11:0] Number of lines masked from the bottom of a frame

8.1.2.4 DAC AND CVBS CONTROL REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
30	DA0	10	-	-	DAC_CLK_INV	RGB_BYPASS	BLANKB	SYNCB	DAC_CKPOL	PD_DAC

DAC_CLK_INV
0 normal (df.)
1 Inverse the digital dac clock

RGB_BYPASS
0 RGB input data go through internal processing
1 RGB input data is bypassed to DAC (df.)

BLANKB BLANK signal to DAC

SYNCB SYNC signal to DAC

DAC_CKPOL
0 normal (df.)
1 inverse the DAC clock polarity

PD_DAC
0 DAC power on (df.)
1 power down the DAC

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
31	DA1	dc	CVBS_BLANK_VAL							

CVBS_BLANK_VAL[7:0] Set the CVBS output blanking level

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
32	DA2	20	CVBS_N_SAV							

CVBS_N_SAV[7:0] Set the CVBS NTSC output SAV position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
33	DA3	20	CVBS_N_EAV							

CVBS_N_EAV[7:0] Set the CVBS NTSC output EAV position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
34	DA4	34	CVBS_P_SAV							

CVBS_P_SAV[7:0] Set the CVBS PAL output SAV position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
35	DA5	18	CVBS_P_EAV							

CVBS_P_EAV[7:0] Set the CVBS NTSC output EAV position

8.1.2.5 OUTPUT SYNC GENERATION REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
38	GC0	00	GCSYNC_EN	-	-	FIELD_IN	GC_INV	GC_XOR	VIN_P	HIN_P

GCSYNC_EN
0 disable gcsync function (df.)
1 enable gcsync function

FIELD_IN
0 progessive input (df.)
1 interlace input

GC_INV
0 no inversion (df.)
1 for GCSYNC output inversion.

GC_XOR
0 GCSYNC AND output (df.)
1 GCSYNC XOR output

VIN_P
0 normal (df.)
1 Inverse the input vertical sync polarity

HIN_P
0 normal (df.)
1 Inverse the input horizontal sync polarity

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
39	GC1	00	H_FALL [11:8]				H_RISE [11:8]			
3A	GC2	00	H_RISE [7:0]							
3B	GC3	00	H_FALL [7:0]							

H_RISE[11:0] Horizontal sync rising edge position

H_FALL[11:0] Horizontal sync falling edge position

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
3C	GC4	00	-	V_FALL [10:8]			-	V_RISE [10:8]		
3D	GC5	00	V_RISE [7:0]							
3E	GC6	00	V_FALL [7:0]							

V_RISE[10:0] Vertical rising edge position

V_FALL[10:0] Vertical falling edge position

8.1.2.5 PICTURE ADJUSTMENT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
40	PA0	80	BRIGHTNESS							

BRIGHTNESS[7:0] Brightness adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
41	PA1	80	CONTRAST							

CONTRAST[7:0] Contrast adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
42	PA2	80	SATURATION							

SATURATION[7:0] Saturation adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
43	PA3	20	-	-	HUE					

HUE[5:0] Hue adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
44	PA4	80	R_BRI							

R_BRI[7:0] R channel output brightness adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
45	PA5	80	G_BRI							

G_BRI[7:0] G channel output brightness adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
46	PA6	80	B_BRI							

B_BRI[7:0] B channel output brightness adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
47	PA7	80	R_CON							

R_CON[7:0] R channel output contrast adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
48	PA8	80	G_CON							

G_CON[7:0] G channel output contrast adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
49	PA9	80	B_CON							

B_CON[7:0] B channel output contrast adjustment

8.1.2.6 OUTPUT PATTERN GENERATION CONTROL REGISTER

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
50	PT0	30	PAT_EN	GEN_SYNC	PT_VPOL	PT_HPOL	PAT_MODE			

PAT_EN
0 disable pattern generation (df.)
1 enable pattern generation

GEN_SYNC

0 use original setting for sync length (df.)

1 Use user setting registers (0x51~57) value to generate horizontal/vertical total length and sync length

PT_VPOL output pattern vsync polarity

PT_HPOL output pattern hsync polarity

PAT_MODE[3:0] Setting the pattern mode

0 Pure color

1 Horizontal increment value line

2 Vertical increment value line

3 Boundary and center line

4 Grid line

5 Color bar of horizontal direction

6 Color bar of vertical direction

7 Diagonal line

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
51	PT1	43	PT_HLEN[11:8]				PT_HACT[11:8]			
52	PT2	1F	PT_HLEN[7:0]							
53	PT3	1F	PT_HACT[7:0]							

PT_HLEN[11:0] output horizontal total length

PT_HACT[11:0] output horizontal active length

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
54	PT4	22	PT_VLEN[11:8]				PT_VACT[11:8]			
55	PT5	73	PT_VLEN[7:0]							
56	PT6	53	PT_VACT[7:0]							

PT_VLEN[11:0] output vertical total length

PT_VACT[11:0] output vertical active length

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
57	PT7	00	PT_YVAL[7:0]							
58	PT8	81	PT_YVAL[9:8]				PT_INCVAL			

PT_YVAL[9:0] Set output pattern Y value

PT_INCVAL[7:0] The incremental value of pattern generation

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
59	PT9	01	PT_INTLEN							

PT_INTLEN[7:0] The interval length of pattern increase

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
5A	PTA	0a					PT_CBVAL[9:8]		PT_CRVAL[9:8]	
5B	PTB	00	PT_CBVAL[7:0]							
5C	PTC	00	PT_CRVAL[7:0]							

PT_CBVAL[9:0] Set output pattern CB value

PT_CRVAL[9:0] Set output pattern CR value

9 ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	-0.3	3.6	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	-0.3	3.6	V
Junction Temperature	T_J	-40	125	°C
Storage Temperature	T_{STG}	-55	125	°C
Lead Temperature (Vapor Phase Soldering, 40 Seconds)	T_L	-	215	°C
Electronic Discharge	T_{ESD}	-2000	2000	V

9.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	3.0	3.3	3.6	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	3.0	3.3	3.6	V
Ambient Operation Temperature	T_A	0	-	70	°C
Package Case Temperature	T_A	-	-	115	°C
Total Power Dissipation	P_{TOT}	-	TBA	-	W

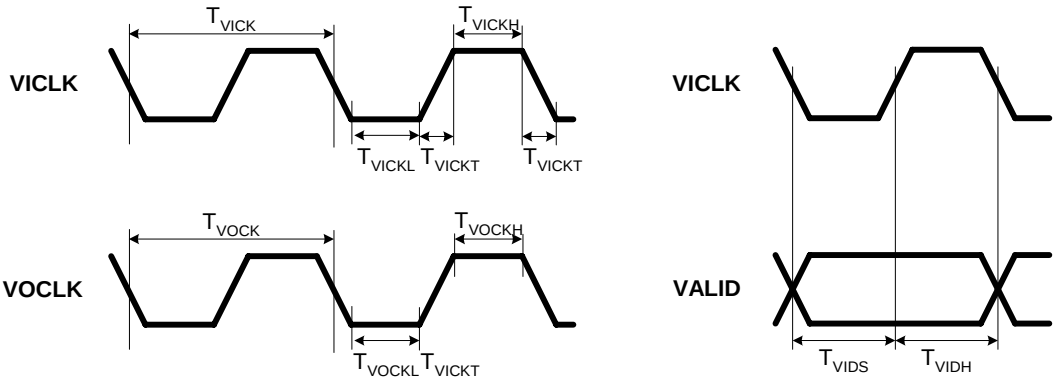
9.3 DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input (I, I_S, I_{PU}, I_{PD})					
High Level Input Voltage	V_{IH}	2	-	3.6	V
Low Level Input Voltage	V_{IL}	-0.3	-	0.8	V
Leakage Current	I_L	-15	-	+10	nA
Output (O_1, O_{TS1})					
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Tri-State Output Leakage Current	I_L	-15	-	+10	nA
Pull-Up/Down Resistor					
Pull-Up Resistor	R_{PU}	-	50	-	KΩ
Pull-Down Resistor	R_{PD}	-	50	-	KΩ

9.4 AC CHARACTERISTICS

9.4.1 VIDEO INTERFACE

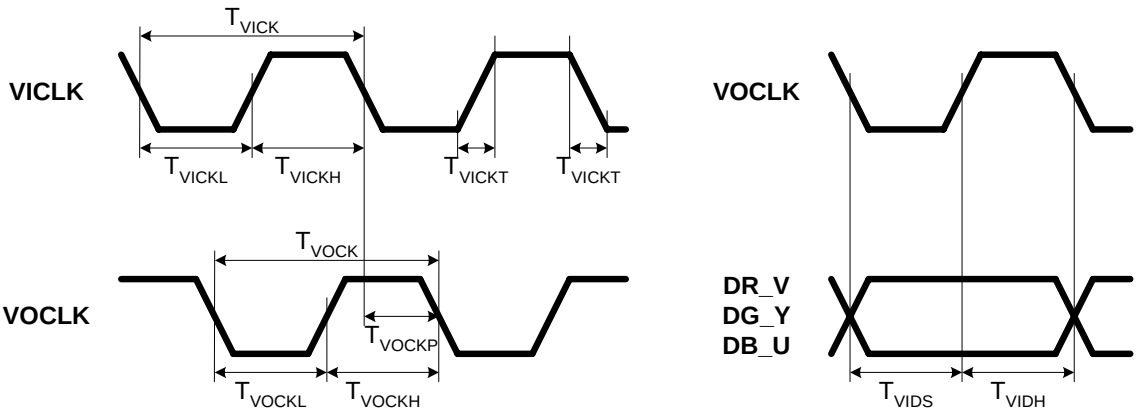
Parameter	Symbol	Min	Typ	Max	Unit
Digital Video Clocks					
Video Input Clock VICLK Frequency	F_{VICK}	0	27	150	MHz
Video Input Clock VICLK Transition Time	T_{VICKT}	-	0.5	-	ns
Video Output Clock VOCLK Frequency	F_{VOCK}	-	27	160	MHz
					ns
Digital Video Input					
Video Input Data Setup Time To VICLK	T_{VIDS}	-	0.5	-	ns
Video Input Data Hold Time From VICLK	T_{VIDH}	-	0.5	-	ns
Digital Video Output					
Video Output Data Delay From VOCLK	T_{VODH}	-	1	-	ns



Digital Video Interface Timing

9.4.2 HOST INTERFACE

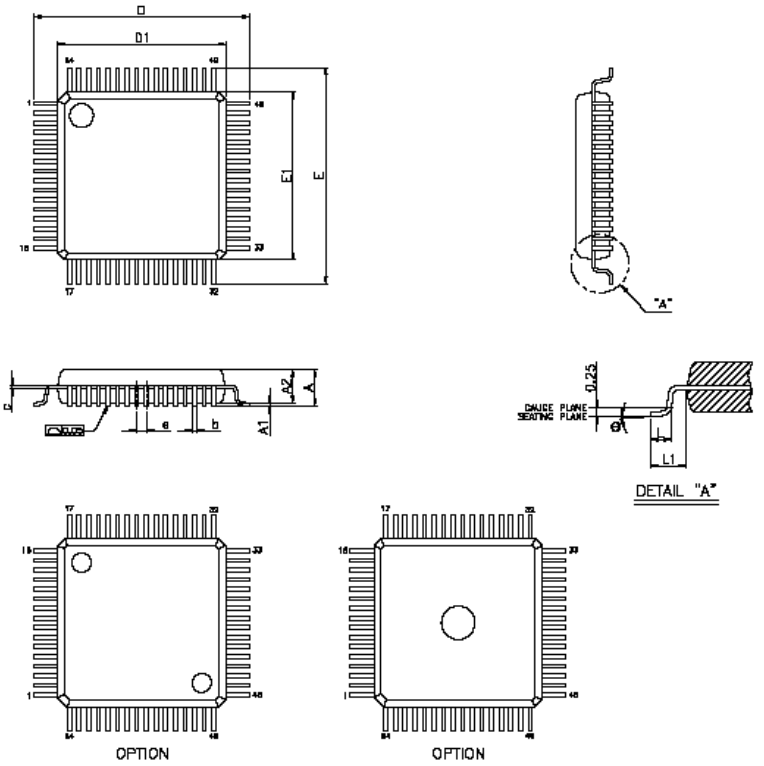
Parameter	Symbol	Min	Typ	Max	Unit
SCL Clock Frequency	F_{SCL}	-	100	-	KHz
Serial Bus Free Time Between STOP and START Condition	T_{BUF}	4.7	-	-	µs
Serial Bus Hold Time For START Condition	T_{HDSTA}	4.0	-	-	µs
SCL Clock Width Low	T_{SCLL}	4.7	-	-	µs
SCL Clock Width High	T_{SCLH}	4.0	-	-	µs
Serial Data Setup Time	T_{HSDS}	0.5	-	-	µs
Serial Data Hold Time	T_{HSDH}	-	-	0	µs
Serial Bus Setup Time For STOP Condition	T_{SUSTO}	4.0	-	-	µs



Digital Video Interface Timing

10 PACKAGE

10.1 VS9126 64PIN-LQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. JEDEC OUTLINE : MS-026 BBD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.