VS2828

USB2.0 / USB3.0

Video Bridge

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1 OVERVIEW

1.1 FEATURES

- Compliant with USB Video Class 1.5 standard
- Compliant with USB Audio Class 1.0 standard
- Built-in USB3.0 SuperSpeed and USB2.0 High-Speed and Full-Speed transceiver
- Support two endpoints (can be programmed to ISO-in or Bulk-in type) for video data to PC
- Support one ISO-in endpoint for audio recording
- Built-in 8032 micro controller
- Maximum CPU clock rate is 48 MHz
- Audio functions
  - Support I2S interface
- Video data output format
  - USB Video Class uncompressed YUY2 payload
  - USB Video Class MJPEG payload (MJPEG UV422)
- Maximum Frame Rates in USB3.0 SuperSpeed Mode
- Maximum Frame Rates in USB2.0 High-speed Mode
- Built-in system PLL for Internal clock generation with Input Crystal Frequency of 24MHz.
- Built-in audio PLL for audio clock generation with Input Crystal Frequency of 24MHz.
- PWM function embedded
- Built-in brown-out circuit (LVD)
- Package and Power
  - 88-pin QFN
  - 1.3V for VS2828 core
  - 3.3V for VS2828 IO
  - 1.8V or 3.3V for sensor interface
  - Lead-free/ Halogen-free/ RoHS/ REACH compliant

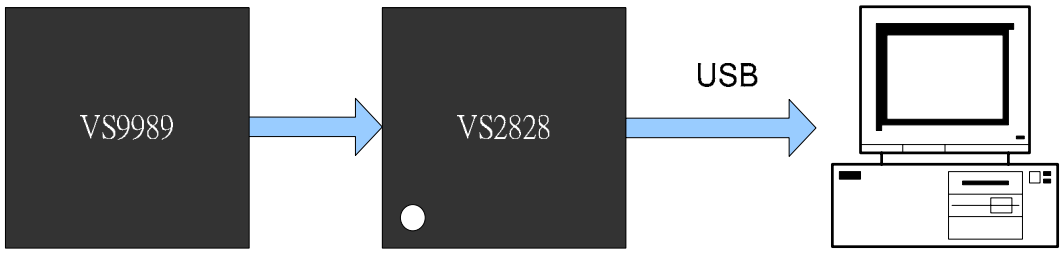
1.2 MAXIMUM FRAME RATES IN USB3.0 SUPERSPEED MODE

Maximum Frame Rate	Full HD (1920x1080)	SXGA (1280x1024)	HD (1280x720)	VGA (640x480)
Non-compressed (YUY2)	60 fps	60 fps	120 fps	120 fps

1.3 MAXIMUM FRAME RATES IN USB2.0 HIGHSPEED MODE

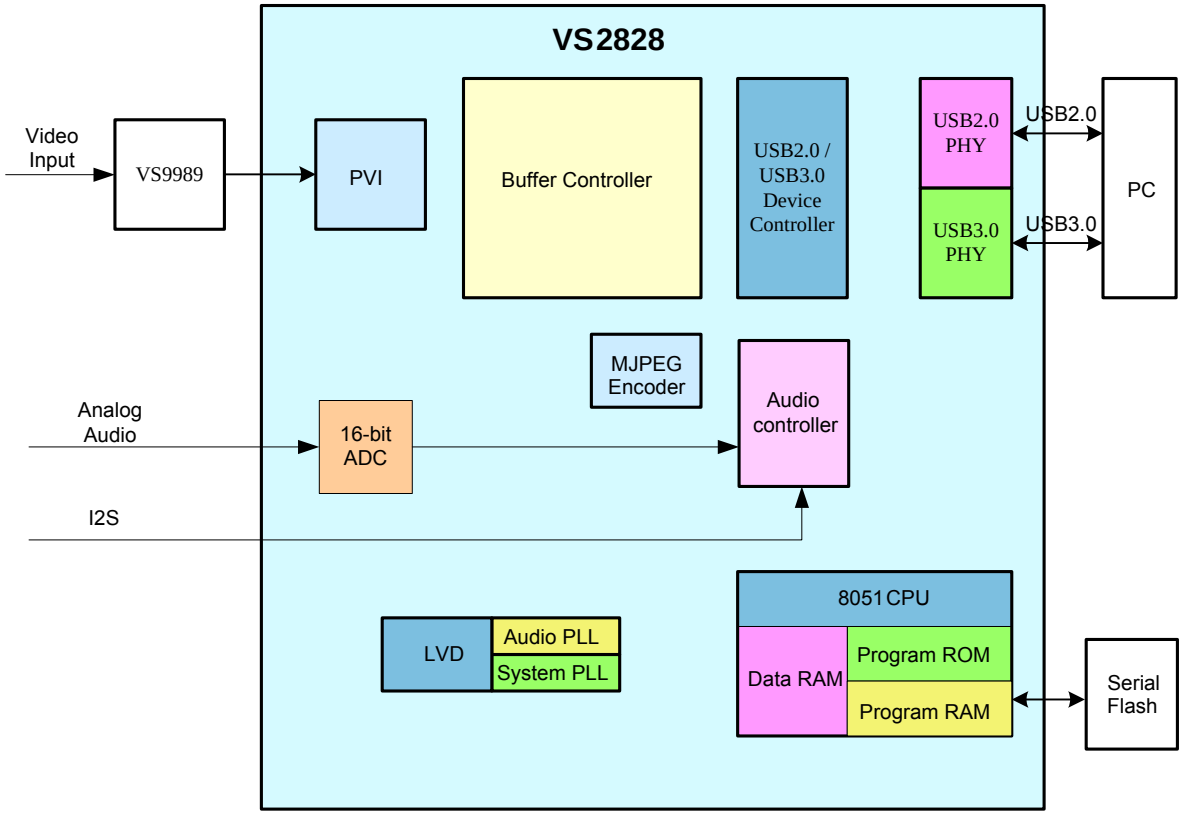
Maximum Frame Rate	Full HD (1920x1080)	SXGA (1280x1024)	HD (1280x720)	VGA (640x480)
Compressed (MJPG)	60 fps	60 fps	120 fps	120 fps

2 USB2.0/USB3.0 VIDEO BRIDGE APPLICATION



3 BLOCK DIAGRAM

The following diagram shows functional blocks and the data flow in the VS2828



4 PIN ASSIGNMENT

4.1 PIN DESCRIPTION (QFN88)

No.	Pin Name	Pin Type	Description
Power domain: OVDD1			
28	XPRSTNN	OD	Power on reset pin, active low. It is open-drain after reset. Reset (low level) comes from VS2828. External circuit must provide pull-up function.
29	XSPISCLK	I	SPI external master clock
30	XSPISDO	O	SPI slave data output
31	XSPISDI	I	SPI slave data input
32	XSPISCSN	I	The external SPI master enable this SPI slave
33	XHIGHDRV	B	GPIO pin, 5V tolerance, 16mA driving current, Support PWM0.
34	XGPIO[5]	B	GPIO pin, reserved for pulse counter 2, I2C clock pin and PWM5
35	OVDD1	DP	IO buffer power, connected to 3.3V power.
36	DVDD	DP	Digital core power, connected to 1.3V power.
37	DVSS	DG	Digital Ground
Power domain: SVDD			
38	XGPIO8	B	Suggest to use as sensor reset control
39	XGPIO9	B	Suggest to use as sensor power down control
40	XSDA	B	Data pin of I2C bus
41	XPCLK	I	Pixel clock from the sensor
42	XSCL	O	Clock of I2C bus
43	XMCLK	O	Master clock for the sensor
44	SVDD	DP	Sensor interface IO buffer power, connected to 3.3V/1.8V power.
45	XRGB[0] / XD1INP	I	Sensor parallel data input bit 0 (**Default , RAW data sensor**)
		B	GPIO. (YUV sensor)
		I	Sensor MIPI data lane1 positive input (MIPI sensor)
46	XRGB[1] / XD1INN	I	Sensor parallel data input bit 1 (**Default , RAW data sensor**)
		B	GPIO. (YUV sensor)
		I	Sensor MIPI data lane1 negative input (MIPI sensor)

47	XRGB[2] / XD2INP	I	Sensor parallel data input bit 2 (Default , RAW data sensor)
		I	Sensor parallel data input bit 0 (YUV sensor)
		I	Sensor MIPI data lane2 positive input (MIPI sensor)
48	XRGB[3] / XD2INN	I	Sensor parallel data input bit 3 (Default , RAW data sensor)
		I	Sensor parallel data input bit 1 (YUV sensor)
		I	Sensor MIPI data lane2 negative input (MIPI sensor)
49	XRGB[4] / XCINP	I	Sensor parallel data input bit 4 (Default , RAW data sensor)
		I	Sensor parallel data input bit 2 (YUV sensor)
		I	Sensor MIPI clock lane positive input (MIPI sensor)
50	XRGB[5] / XCINN	I	Sensor parallel data input bit 5 (Default , RAW data sensor)
		I	Sensor parallel data input bit 3 (YUV sensor)
		I	Sensor MIPI clock lane negative input (MIPI sensor)
51	XRGB[6] / XD3INP	I	Sensor parallel data input bit 6 (Default, RAW data sensor)
		I	Sensor parallel data input bit 4 (YUV sensor)
		I	Sensor MIPI data lane3 positive input (MIPI sensor)
52	XRGB[7] / XD3INN	I	Sensor parallel data input bit 7 (Default , RAW data sensor)
		I	Sensor parallel data input bit 5 (YUV sensor)
		I	Sensor MIPI data lane3 negative input (MIPI sensor)
53	XRGB[8] / XD4INP	I	Sensor parallel data input bit 8 (Default , RAW data sensor)
		I	Sensor parallel data input bit 6 (YUV sensor)
		I	Sensor MIPI data lane4 positive input (MIPI sensor)
54	XRGB[9] / XD4INN	I	Sensor parallel data input bit 9 (Default, RAW data sensor)
		I	Sensor parallel data input bit 7 (YUV sensor)
		I	Sensor MIPI data lane4 negative input (MIPI sensor)
55	XHSYNC / XC2INP	I	Sensor horizontal synchronization signal (Default, Parallel sensor)
		I	Sensor MIPI clock lane positive input for the second interface
56	XVSYNC / XC2INN	I	Sensor vertical synchronization signal (Default, Parallel sensor)
		I	Sensor MIPI clock lane negative input for the second interface
57	XD3_2INP	I	Another MIPI data lane3 positive input
58	XD3_2INN	I	Another MIPI data lane3 negative input
59	MVDD	AP	MIPI interface power (1.3V/1.8V)
Power domain: SVDD2			

60	XMCLK2	O	Master clock for the sensor 2
61	SVDD2	DP	Sensor 2 interface IO buffer power, connected to 3.3V/1.8V power.
62	XSCL2	O	Clock of I2C bus for the sensor 2
63	XSDA2	B	Data pin of I2C bus for the sensor 2
64	XGPIO11	B	Suggest to use as sensor 2 power down control and PWM4
Power domain: AVDD			
65	XVREF	AP_OUT	Reference voltage for 16-bit ADC. Voltage level is 0.5*AVDD
66	XMICBIAS	AP_OUT	Buffered voltage output suitable for microphone biasing. Voltage level is 0.75*AVDD
67	XMICINLN	A	Left channel microphone negative/single-ended input
68	XMICINLP	A	Left channel microphone positive input
69	AVDD	AP	Analog power, connected to 3.3V power. (Power of 16-bit ADC)
70	AVSS	AG	Analog ADC ground
Power domain: OVDD2			
71	XIIS_ADCBCLK	O	Clock output for digital microphone
		B	I2S bit clock for recording **(Default)**
72	XIIS_ADCLRC	B	I2S left / right channel selection for recording
73	XIIS_ADCDAT	I	Data input for digital microphone
		I	I2S recording data **(Default)**
74	XSO	B	Serial Flash data out / EEPROM I2C data pin
75	XCEB	O	Serial Flash Chip enable
76	XSI	O	Serial Flash data input
77	XESK	O	Serial Flash clock input / EEPROM I2C clock pin
78	XIIS_ADCMCLK	O	I2S master clock for recording
79	XCGPIO[0]	B	TX of RS232 in standard 8032. CPU. Default GPIO function and PD enabled.
80	OVDD2	DP	IO buffer power, connected to 3.3V power.
81	DVDD	DP	Digital core power, connected to 1.3V power.
82	XGPIO[1]	B	GPIO pin, reserved for PWM1
83	XGPIO[2]	B	GPIO pin, reserved for PWM2
84	XGPIO[3]	B	GPIO pin, reserved for I2C data pin and PWM3

85	XGPIO[4]	B	GPIO pin, reserved for pulse counter 1, I2C clock pin and PWM4
Power domain: AVDD_MTX			
86	DVDD_MTX	AP	1.3V core power for MIPI TX
87	XMTXD3N	O	MIPI TX data lane 3, differential negative output
88	XMTXD3P	O	MIPI TX data lane 3, differential positive output
1	XMTXD2N	O	MIPI TX data lane 2, differential negative output
2	XMTXD2P	O	MIPI TX data lane 2, differential positive output
3	XMTXCKN	O	MIPI TX clock lane, differential negative output
4	XMTXCKP	O	MIPI TX clock lane, differential positive output
5	XMTXD1N	O	MIPI TX data lane 1, differential negative output
6	XMTXD1P	O	MIPI TX data lane 1, differential positive output
7	XMTXD0N	O	MIPI TX data lane 0, differential negative output
8	XMTXD0P	O	MIPI TX data lane 0, differential positive output
9	DVSS_MTX	AG	Ground for MIPI TX
10	VREF_MTX	AP_OUT	0.4V analog power for HS TX DRIVER. Connect to capactor 1uF & 0.1uF
11	AVDD_MTX	AP	3.3V analog power for MIPI TX
Power domain: UAVDD			
12	XDP	B	USB2.0 D+ pin
13	XDM	B	USB2.0 D- pin
14	XRREF	A	USB reference resistor connection. Attach a 200Ω +-1% 100-ppm/C precision resistor to ground.
15	UDVDD	AP	USB core power supply 1.3V
16	UAVDD	AP	USB analog power supply 3.3V
17	UVSS	AG	USB analog ground
18	XTXM	O	USB3.0 TX- pin
19	XTXP	O	USB3.0 TX+ pin
20	XRXM	I	USB3.0 RX- pin
21	XRXP	I	USB3.0 RX+ pin
22	UVSS	AG	USB analog ground
Power domain: XVDD			
23	PVDD	AP	PLL power (3.3V power)
24	XVDD	AP	Crystal power (1.3V power)
25	XTALO	O	Crystal clock output pad

26	XTALI	I	Crystal 24MHz clock input pad
27	XVSS	AG	Crystal and PLL ground

Note: Please also refer to section 7.2 to find the voltage specification for all power supplies.

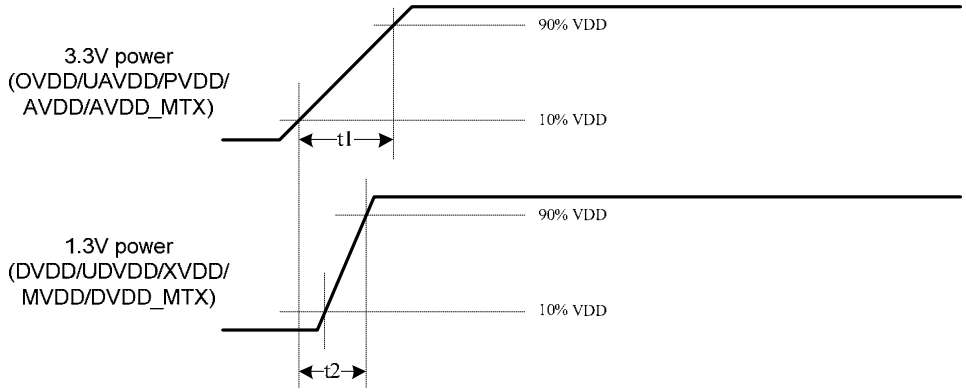
4.2 IO-TRAP PINS

Some configurations must be determined right after the chip is powered on. The VS2828 adopts an IO-trap mechanism to do such configurations and they are not changed during the operation of the VS2828. While using the IO-trap mechanism, the VS2828 samples the signal states on the "**IO-Trap pins**" ("**XCGPIO[0], XGPIO[1], XGPIO[2]**") during the power-on reset period and then, in turn, sets internal configurations based on these sampled values. The IO-trap pins should be pulled high or low for different configurations. In particular, "**IO-Trap pins**" are internally pulled down for default configurations. For details of all the IO-trap settings in the VS2828, please see the following table.

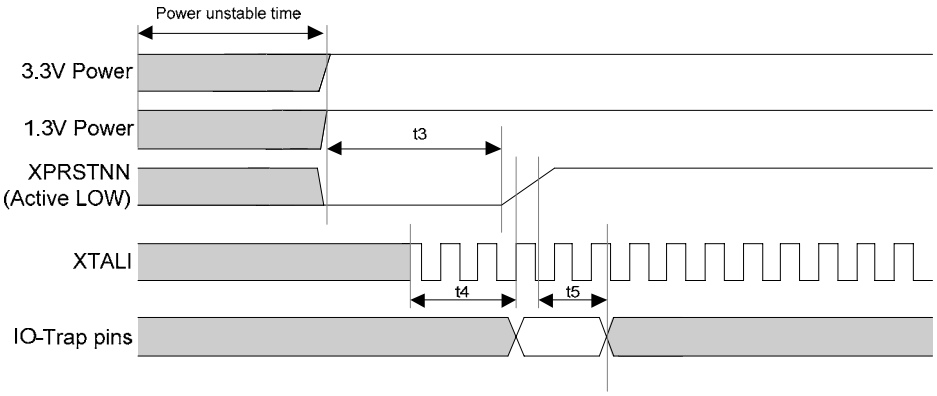
IO-trap	Corresponding Pins	Name	Description
IO-trap[1]	XGPIO[1]	Testmode	1'b0: Normal operation. **1'b1: Not allowed.**
IO-trap[2]	XGPIO[2]	Cpucfg	1'b0: Enable internal ROM 1'b1: Enable external ROM (or flash memory). This is for MCM package application.
RSV-trap[0]	XCGPIO[0]	FastRst	1'b0: Normal operation. **1'b1: Not allowed.**

4.3 POWER ON SEQUENCE AND IO TRAPPING

To power on the chip, the 3.3V (IO) power and 1.3V (core) power require to meet the rise time, t1 and delay time, t2, as the following figure. The rise time is defined as the time between the 10% and 90% of the 3.3V power. The delay time is defined as the time between the 10% of 3.3V power and 90% of the 1.3V power. Please refer to section 7.2 for the 3.3V and 1.3V voltage specification.



The power-on reset timing is shown below. As in the timing, the 3.3V power and 1.3V power should be ready first. The "**XPRSTNN**" (power-on reset pin), which connects to an internal LVD / POR circuits and Schmitt-Triggered buffer, will assert for 3 ms (t3) after both the 3.3V power and the 1.3V power are ready. Before the dessert of the "**XPRSTNN**", the external crystal clock (through "**XTALI**" pin) should be ready at least 100us (t4). At the rising edge of **"XPRSTNN**", VS2828 latches the value of the "**IO-Trap pins**" ("**XCGPIO[0], XGPIO[1], XGPIO[2]**") to determine the IO-TRAP configurations. The "**IO-Trap pins**" must be stable in order to meet the t5 (IO-Trap hold time) requirement. If latching incorrect values, VS2828 will not be able to function normally.



Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	3.3V rising time	-	-	2	ms
t2	3.3V to 1.3V delay time	0	-	2	ms
t3	LVD reset time	2.4	3	3.6	ms
t4	Crystal clock stable time	100	-	-	us
t5	IO-Trap hold time	15	-	-	us

5 ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 7.1 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_T	-0.5 to 4.0	V
Supply Voltage relative to VSS	V_{DD}	-0.5 to 4.0	V
Ambient Temperature	T_{OPT}	0 to 70	°C
Storage Temperature	T_{STG}	-55 to 125	°C

5.2 DC CHARACTERISTICS

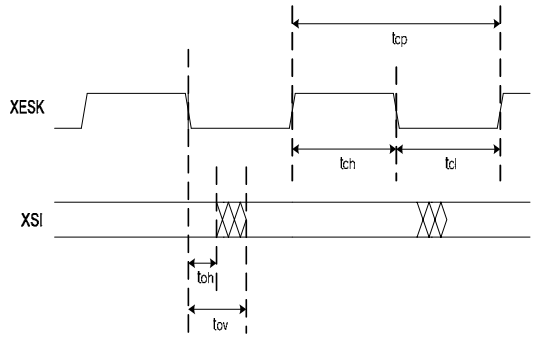
Table 7.2 DC Characteristics (T_A＝25℃)

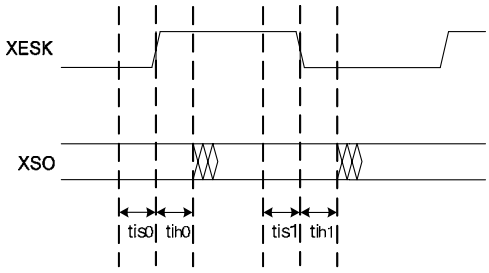
Symbol	Parameter	Min.	Typ.	Max.	Unit
OVDD1	Digital I/O operating voltage	3.07	3.3	3.6	V
OVDD2	Digital I/O operating voltage	3.07	3.3	3.6	V
DVDD	Digital core operating voltage	1.235	1.3	1.32	V
SVDD	Sensor interface voltage	1.62 / 3.07	1.8 / 3.3	1.98 / 3.6	V
SVDD2	2nd Sensor interface voltage	1.62 / 3.07	1.8 / 3.3	1.98 / 3.6	V
AVDD	Audio ADC operation voltage	3.07	3.3	3.6	V
AVDD_MTX	MIPI TX IO voltage	3.07	3.3	3.6	V
DVDD_MTX	MIPI TX core voltage	1.235	1.3	1.32	V
UAVDD	USB IO voltage	3.07	3.3	3.6	V
UDVDD	USB core voltage	1.235	1.3	1.32	V
PVDD	PLL operating voltage	3.07	3.3	3.6	V
XVDD	Crystal operating voltage	1.235	1.3	1.32	V
MVDD	MIPI RX operating voltage	1.235 / 1.62	1.3 / 1.8	1.32 / 1.98	V
I_{sup}	Chip suspend current @ HS mode (3.3V total)	-	-	1.4	mA
I_{sup}	Chip suspend current @ SS mode (3.3V	-	-	2.45	mA

Symbol	Parameter	Min.	Typ.	Max.	Unit
	total)				
I_{op}	Chip operation current (operation in USB HS mode with FHD image) (3.3V total)	-	-	120	mA
I_{op}	Chip operation current (operation in USB SS mode with 8M image) (3.3V total)	-	-	250	mA
$V_{IH(3.3V)}$	3.3V IO Input high voltage	2.00	-	-	V
$V_{IH(1.8V)}$	1.8V IO Input high voltage	1.17	-	-	V
$V_{IL(3.3V)}$	3.3V IO Input low voltage	-	-	0.8	V
$V_{IL(1.8V)}$	1.8V IO Input low voltage	-	-	0.63	V
V_{T+}	Schmitt trigger positive-going threshold	1.49	1.57	1.64	V
V_{T-}	Schmitt trigger negative-going threshold	1.07	1.14	1.20	V
I_{IL}	Input leakage current	-	-	1	μA
R_d(3.3V)	3.3V IO Pull down resistor	53K	79K	129K	Ω
R_d(1.8V)	1.8V IO Pull down resistor	113K	185K	312K	Ω
I_{OH} (4mA)	4mA IO output high current@ V_{OH} = 2.4 V	10.1	19.7	31.8	mA
I_{OL} (4mA)	4mA IO output low current@ V_{OL} = 0.4 V	7.3	11.9	17.2	mA
I_{OH} (8mA)	8mA IO output high current@ V_{OH} = 2.4 V	18.1	35.2	57.4	mA
I_{OL} (8mA)	8mA IO output low current@ V_{OL} = 0.4 V	14.5	24	34.6	mA
I_{OH} (12mA)	12mA IO output high current@ V_{OH} = 2.4 V	23.2	45.1	73.0	mA
I_{OL} (12mA)	12mA IO output low current@ V_{OL} = 0.4 V	19.0	31.1	44.9	mA
I_{OH} (16mA)	16mA IO output high current@ V_{OH} = 2.4 V	33.0	64.3	104.2	mA
I_{OL} (16mA)	16mA IO output low current@ V_{OL} = 0.4 V	23.0	35.6	48.3	mA
R_{ref}	USB reference resistor	198	200	202	Ω
V_{LVD}	LVD reset voltage	2.565	2.7	2.835	V

5.3 AC CHARACTERISTICS

5.3.1 SERIAL FLASH INTERFACE TIMING





Symbol	Parameter	Min.	Max.	Unit
tcp	Clock period	22.72 @44MHz	-	ns
tch	Clock high time	11.36 @44MHz	-	ns
tcl	Clock low time	11.36 @44MHz	-	ns
tov	Clock to output valid	-	6	ns
toh	Output hold time	0	-	ns
tis0 *1	Data in setup time of sample mode 0	2	-	ns
tih0 *1	Data in hold time of sample mode 0	2	-	ns
tis1 *2	Data in setup time of sample mode 1	2	-	ns
tih1 *2	Data in hold time of sample mode 1	2	-	ns

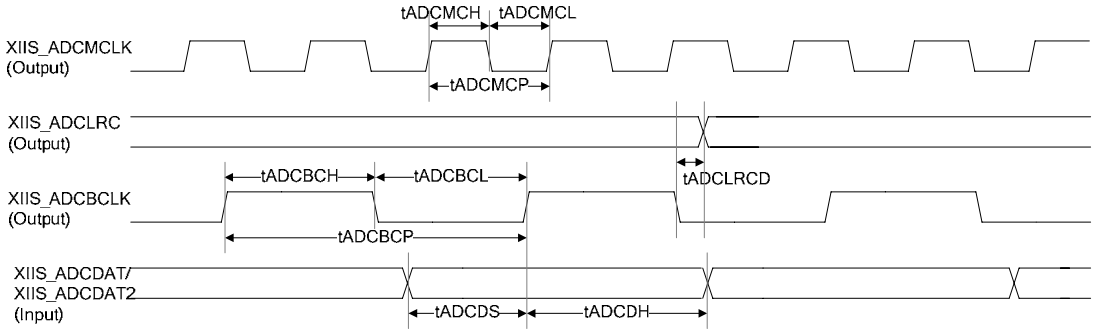
*1: Sample mode determines the sampling edge of XESK

Mode 0: Sample at rising edge of XESK

Mode 1: Sample at falling edge of XESK

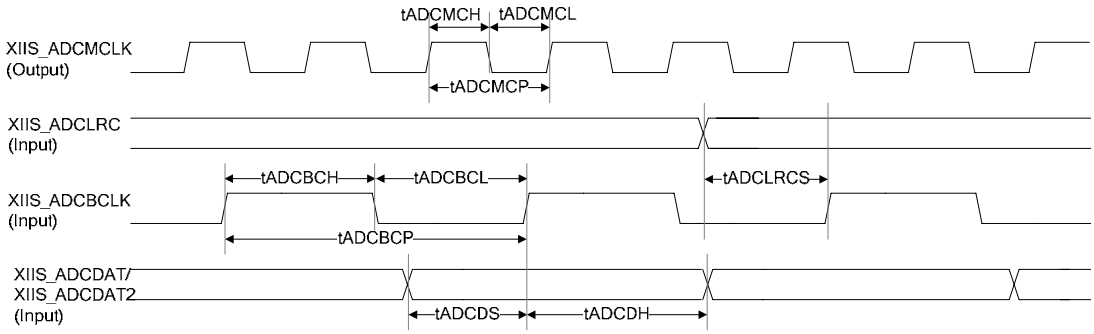
5.3.2 AUDIO INTERFACE TIMING

IIS Recording Timing (Master mode)



Symbol	Parameter	Min.	Typ.	Max.	Unit
tADCMCP	XIIS_ADCMCLK period	81.38	-	-	ns
tADCMCH	XIIS_ADCMCLK high pulse width	32	-	-	ns
tADCMCL	XIIS_ADCMCLK low pulse width	32	-	-	ns
tADCBCP	XIIS_ADCBCLK period	162.76	-	-	ns
tADCBCH	XIIS_ADCBCLK high pulse width	65	-	-	ns
tADCBCL	XIIS_ADCBCLK low pulse width	65	-	-	ns
tADCLRCD	XIIS_ADCLRC propagation delay from XIIS_ADCBCLK alling edge	-	-	10	ns
tADCDS	XIIS_ADCDAT/XIIS_ADCDAT2 setup time to XIIS_ADCBCLK rising edge	10	-	-	ns
tADCDH	XIIS_ADCDAT/XIIS_ADCDAT2 hold time from XIIS_ADCBCLK rising edge	65	-	-	ns

IIS Recording Timing (Slave mode)



Symbol	Parameter	Min.	Typ.	Max.	Unit
tADCMCP	XIIS_ADCMCLK period	81.38	-	-	ns
tADCMCH	XIIS_ADCMCLK high pulse width	32	-	-	ns
tADCMCL	XIIS_ADCMCLK low pulse width	32	-	-	ns
tADCBCP	XIIS_ADCBCLK period	162.76	-	-	ns
tADCBCH	XIIS_ADCBCLK high pulse width	65	-	-	ns
tADCBCL	XIIS_ADCBCLK low pulse width	65	-	-	ns
tADCLRCS	XIIS_ADCLRC setup time to XIIS_ADCBCLK rising edge	10	-	-	ns
tADCDS	XIIS_ADCDAT/XIIS_ADCDAT2 setup time to XIIS_ADCBCLK rising edge	10	-	-	ns
tADCDH	XIIS_ADCDAT/XIIS_ADCDAT2 hold time from XIIS_ADCBCLK rising edge	65	-	-	ns

Mono ADC Specifications

Power Consumption Electrical Characteristics

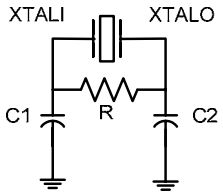
(TA=25°C, AVDD=3.3V, DVDD=1.3V, Clock MCLKAD =12.288MHz)

Parameter		Min	Typ	Max	Unit
Reference voltage (VREF)		-	*0.5* AVDD*	-	*V*
ADC supply current	ADC operating (see Note 2)	-	5	-	mA
ADC power dissipation	ADC operating (see Note 2)	-	16.5	-	mW
ADC supply current	ADC power down (see Note 3)	-	-	1	uA
ADC power dissipation	ADC power down (see Note 3)	-	-	3.3	uW

NOTE 2: PDAD and PDMICBIAS are "Low".

NOTE 3: PDAD and PDMICBIAS are "High".

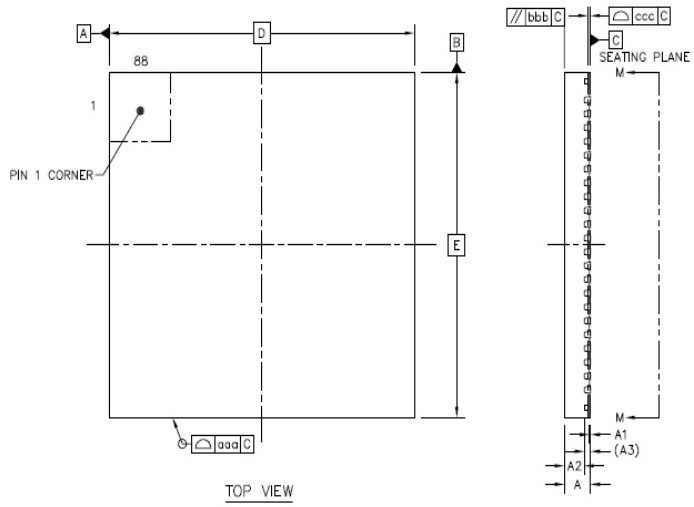
5.4 CRYSTAL SPECIFICATIONS

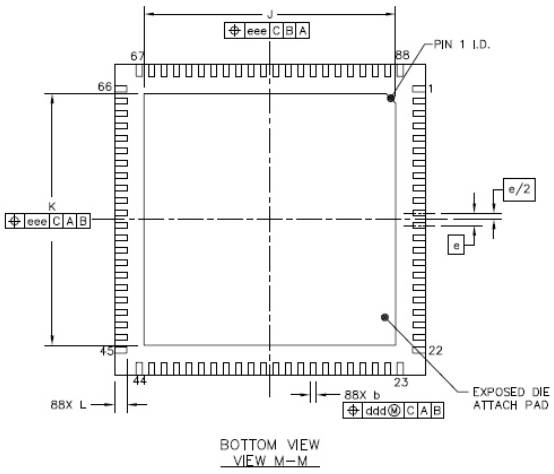


Parameter	Min.	Typ.	Max.	Unit
Clock Frequency (F)	-	24	-	Mhz
Resistor (R)	-	300	-	KΩ
Capacitor (C1)	-	12	-	pF
Capacitor (C2)	-	12	-	pF

6 PACKAGE INFORMATION

6.1 QFN88 OUTLINE DRAWING AND PACKAGE INFORMATION





Symbol	QFN88		
	Min.	Nom.	Max.
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	-	0.65	0.67
A3	0.203 REF.		

Symbol	QFN88		
	Min.	Nom.	Max.
b	0.15	0.20	0.25
D	10 BSC.		
E	10 BSC.		
e	0.4 BSC.		
J	8.0	8.1	8.25
K	8.0	8.1	8.25
L	0.30	0.40	0.50
aaa	0.1		
bbb	0.1		
ccc	0.08		
ddd	0.1		
eee	0.1		

Unit: Millimeter

6.2 ORDERING INFORMATION

Product Number	Package Type	Memo
VS2828-HV361	QFN 88-pin Green Package	Pitch: 0.4mm Body size: 10mm*10mm*0.85mm

6.3 STORAGE CONDITION AND PERIOD FOR PACKAGE

For Green Packages:

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the “CAUTION Note” on dry pack bag.

6.4 RECOMMENDED SMT TEMPERATURE PROFILE

This “Recommended” temperature profile is a rough guideline for SMT processing reference. Most of SUNPLUS MMEDIA leadframe-based products choose Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) products with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.