## Features

- Precision voltage monitor for 3V, 3.3V or 5V power supplies
- Reset remains valid with $V_{CC}$ as low as 1V
- 140ms minimum reset pulse width available
- 3μA typical supply current
- Available in 4-pin SOT-143 package

## Applications

- Computer
- Controller
- Intelligent Instruments
- Critical uP and uC Power Monitoring
- Portable/Battery-Powered Equipment

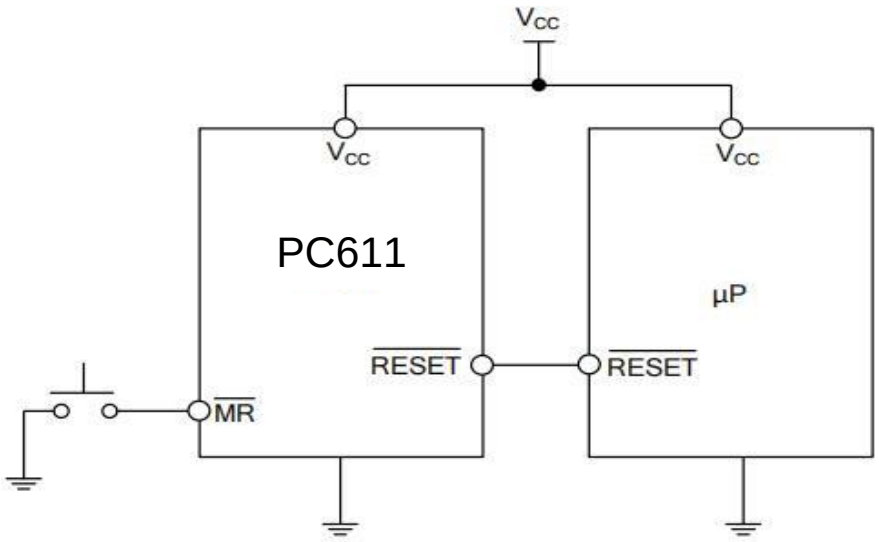
## Description

The PC611is a low-power microprocessor (μP) supervisory circuit used to monitor power supplies in microprocessor and digital systems. Low supply current makes the PC611ideal for use in portable equipment. The device comes in a 4-pin SOT-143 package.

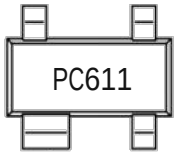
The PC611provides excellent circuit reliability and low BOM cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits. The PC611also provides a debounced manual reset input.

The function of this device is to assert a reset if either the power supply drops below a designed reset threshold level or $\overline{MR}$ is forced low. The reset comparator is designed to ignore fast transients on $V_{CC}$. Reset thresholds are available for operation with a variety of supply voltages.

## Typical Application Circuit

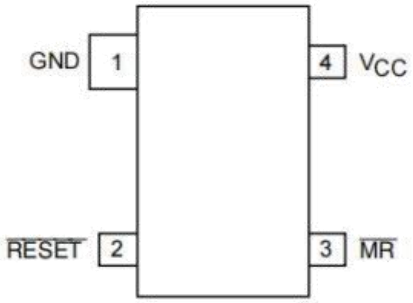


# Ordering and Marking Information

| Part Number | Marking Code | package |
|---|---|---|
| PC611 |  <br>PC611= Device code<br>X=Special Code | **SOT-143** |

# Pin Configuration

SOT-143(TOP VIEW)



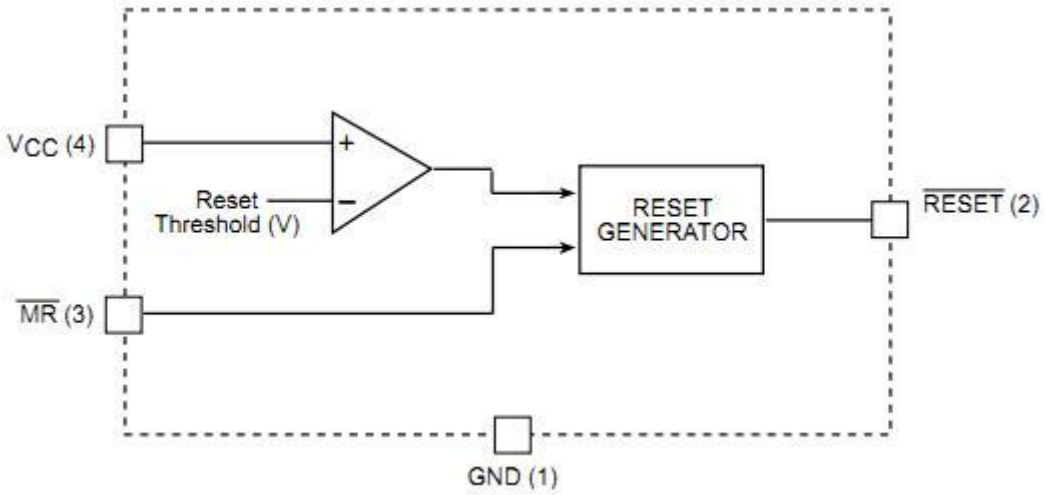

# Pin Description

| Pin No. | Name | Function |
|---|---|---|
| 1 | GND | IC Ground Pin. |
| 2 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ goes low if $V_{CC}$ falls below the reset threshold and remains asserted for one reset timeout period after $V_{CC}$ exceeds the reset threshold. |
| 3 | $\overline{\text{MR}}$ | Manual Reset Input. A logic low on $\overline{\text{MR}}$ forces a reset timeout period after $\overline{\text{MR}}$ goes high. This input can be shorted to ground via a switch or driven from CMOS or TTL logic. Float if unused. |
| 4 | $V_{CC}$ | Power Supply Input. |

# Absolute Maximum Values

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Terminal Voltage($V_{CC}$) | $V_{CC}$ | -0.3 to 6.0V | V |
| Input Current( $V_{CC}$,$\overline{MR}$) | $V_{CC}$, $\overline{MR}$ | 20 | mA |
| Output Current($\overline{RESET}$) | $\overline{RESET}$ | 20 | mA |
| ESD Rating | | 3 | KV |
| Lead Temperature(soldering,10sec) | | 300 | ℃ |
| Junction Temperature | | 150 | ℃ |
| Storage Temperature | | -65 to 160 | ℃ |
| Junction Temperature | | 150 | ℃ |
| Storage Temperature | | -65 to 150 | ℃ |
| SOT-143 Package Thermal Resistance | $R_{\theta JA}$ | 250 | ℃/W |
| SOT-143 Package Thermal Resistance | $R_{\theta JC}$ | 115 | ℃/W |

# Functional Diagram



# Electrical Characteristics

PC611-**T(3.08) (TA = +25℃ unless otherwise stated, VCC = 5.0V)**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operation Voltage Range | $V_{CC}$ | 1 | | 5.5 | V | $T_A$=-40℃ to 85℃ |
| Supply Current | $I_{CC}$ | | 3 | 8 | μA | $V_{CC}$=3.3V, no load |
| Reset Voltage Threshold | $V_{TH}$ | 3 | 3.08 | 3.15 | V | |
| Reset Timeout Period | $t_{RST}$ | 140 | | 560 | ms | |
| $\overline{RESET}$ Output Voltage | $V_{OH}$ | 0.8×$V_{CC}$ | | | V | $I_{SOURECE}$=500μA |
| | $V_{OL}$ | | | 0.3 | V | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=1.2mA |
| | | | | 0.3 | V | $V_{CC}$>1V,$I_{SINK}$=50μA, $T_A$=-40℃ to 85℃ |
| $\overline{MR}$ Minimum Pulse Width | | 10 | | | μs | |
| $\overline{MR}$ to Reset Delay | | | 0.5 | | μs | |
| $\overline{MR}$ Input Threshold | $V_{IH}$ | 0.7×$V_{CC}$ | | | V | |
| | $V_{IL}$ | | | 0.25×$V_{CC}$ | V | |
| $\overline{MR}$ Pull-Up resistance | | 10 | 20 | 30 | kΩ | |
| $\overline{MR}$ Glitch Immunity | | | 100 | | ns | |

PC611-**M(4.38) ($T_A$ = +25℃ unless otherwise stated, VCC = 5.0V)**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operation Voltage Range | VCC | 1 | | 5.5 | V | $T_A$=-40℃ to 85℃ |
| Supply Current | ICC | | 3 | 8 | μA | $V_{CC}$=3.3V, no load |
| Reset Voltage Threshold | $V_{TH}$ | 4.25 | 4.38 | 4.50 | V | |
| Reset Timeout Period | $t_{RST}$ | 140 | | 560 | ms | |
| $\overline{RESET}$ Output Voltage | $V_{OH}$ | 0.8×VCC | | | V | $I_{SOURECE}$=500μA |
| | $V_{OL}$ | | | 0.3 | V | $V_{CC}$=VTH min, $I_{SINK}$=1.2mA |
| | | | | 0.3 | V | $V_{CC}$>1V,$I_{SINK}$=50μA, $T_A$=-40℃ to 85℃ |
| $\overline{MR}$ Minimum Pulse Width | | 10 | | | μs | |
| $\overline{MR}$ to Reset Delay | | | 0.5 | | μs | |
| $\overline{MR}$ Input Threshold | $V_{IH}$ | 0.7×VCC | | | V | |
| | $V_{IL}$ | | | 0.25×VCC | V | |
| $\overline{MR}$ Pull-Up resistance | | 10 | 20 | 30 | kΩ | |
| $\overline{MR}$ Glitch Immunity | | | 100 | | ns | |

PC611-**L(4.63) ($T_A$ = +25℃ unless otherwise stated, VCC = 5.0V)**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operation Voltage Range | $V_{CC}$ | 1 | | 5.5 | V | $T_A$=-40℃ to 85℃ |
| Supply Current | $I_{CC}$ | | 3 | 8 | μA | $V_{CC}$=3.3V, no load |
| Reset Voltage Threshold | $V_{TH}$ | 4.5 | 4.63 | 4.8 | V | |
| Reset Timeout Period | $t_{RST}$ | 140 | | 560 | ms | |
| $\overline{RESET}$ Output Voltage | $V_{OH}$ | 0.8×$V_{CC}$ | | | V | $I_{SOURECE}$=500μA |
| | $V_{OL}$ | | | 0.3 | V | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=1.2mA |
| | | | | 0.3 | V | $V_{CC}$>1V,$I_{SINK}$=50μA, $T_A$=-40℃ to 85℃ |
| $\overline{MR}$ Minimum Pulse | | 10 | | | μs | |
| $\overline{MR}$ to Reset Delay | | | 0.5 | | μs | |
| $\overline{MR}$ Input Threshold | $V_{IH}$ | 0.7×$V_{CC}$ | | | V | |
| | $V_{IL}$ | | | 0.25×$V_{CC}$ | V | |
| $\overline{MR}$ Pull-Up resistance | | 10 | 20 | 30 | kΩ | |
| $\overline{MR}$ Glitch Immunity | | | 100 | | ns | |

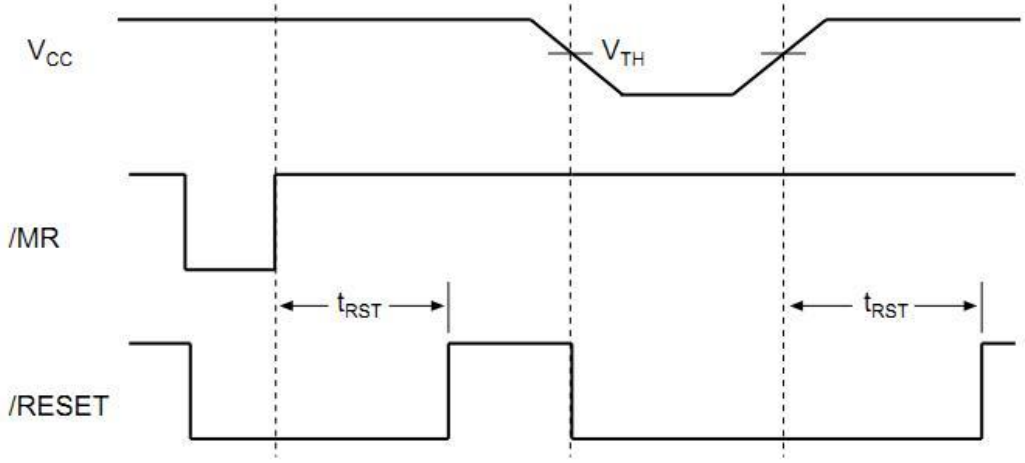
PC611-**S(2.93) (TA = +25℃ unless otherwise stated, VCC = 5.0V)**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operation Voltage Range | $V_{CC}$ | 1 | | 5.5 | V | $T_A$=-40℃ to 85℃ |
| Supply Current | $I_{CC}$ | | 3 | 8 | μA | $V_{CC}$=3.3V, no load |
| Reset Voltage Threshold | $V_{TH}$ | 2.8 | 2.93 | 3.0 | V | |
| Reset Timeout Period | $t_{RST}$ | 140 | | 560 | ms | |
| $\overline{RESET}$ Output Voltage | $V_{OH}$ | 0.8×$V_{CC}$ | | | V | $I_{SOURECE}$=500μA |
| | $V_{OL}$ | | | 0.3 | V | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=1.2mA |
| | | | | 0.3 | V | $V_{CC}$>1V,$I_{SINK}$=50μA, $T_A$=-40℃ to 85℃ |
| $\overline{MR}$ Minimum Pulse | | 10 | | | μs | |
| $\overline{MR}$ to Reset Delay | | | 0.5 | | μs | |
| $\overline{MR}$ Input Threshold | $V_{IH}$ | 0.7×$V_{CC}$ | | | V | |
| | $V_{IL}$ | | | 0.25×$V_{CC}$ | V | |
| $\overline{MR}$ Pull-Up resistance | | 10 | 20 | 30 | kΩ | |
| $\overline{MR}$ Glitch Immunity | | | 100 | | ns | |

PC611-**R(2.63) (TA = +25℃ unless otherwise stated, VCC = 5.0V)**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operation Voltage Range | $V_{CC}$ | 1 | | 5.5 | V | $T_A$=-40℃ to 85℃ |
| Supply Current | $I_{CC}$ | | 3 | 8 | μA | $V_{CC}$=3.3V, no load |
| Reset Voltage Threshold | $V_{TH}$ | 2.58 | 2.63 | 2.68 | V | |
| Reset Timeout Period | $t_{RST}$ | 140 | | 560 | ms | |
| $\overline{RESET}$ Output Voltage | $V_{OH}$ | 0.8×$V_{CC}$ | | | V | $I_{SOURECE}$=500μA |
| | $V_{OL}$ | | | 0.3 | V | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=1.2mA |
| | | | | 0.3 | V | $V_{CC}$>1V,$I_{SINK}$=50μA, $T_A$=-40℃ to 85℃ |
| $\overline{MR}$ Minimum Pulse Width | | 10 | | | μs | |
| $\overline{MR}$ to Reset Delay | | | 0.5 | | μs | |
| $\overline{MR}$ Input Threshold | $V_{IH}$ | 0.7×$V_{CC}$ | | | V | |
| | $V_{IL}$ | | | 0.25×$V_{CC}$ | V | |
| $\overline{MR}$ Pull-Up resistance | | 10 | 20 | 30 | kΩ | |
| $\overline{MR}$ Glitch Immunity | | | 100 | | ns | |

# Timing Diagram




**Reset Timing Diagram**

# Application Information

### Microprocessor Reset

The $\overline{\text{RESET}}$ pin is asserted whenever $V_{CC}$ falls below the reset threshold voltage. The $\overline{\text{RESET}}$ pin remains asserted for a period of 140ms after $V_{CC}$ has risen above the reset threshold voltage. The reset and powers up in a known condition after a power failure. $\overline{\text{RESET}}$ will remain valid with $V_{CC}$ as low as 1V.

### VCC Transients

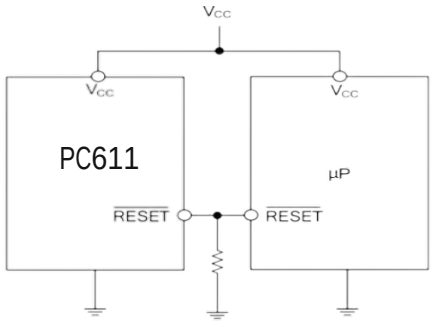
The PC611is relatively immune to negative-going VCC glitches below the reset threshold. Typically, a negative-going transient 125mV below the reset threshold with a duration of 20μs or less will not cause a reset.

### Interfacing to Bidirectional Reset Pins

ThePC611can interface with μPs with bidirectional reset pins by connecting a 4.7kΩ resistor in series with the PC611output and the μP reset pin.

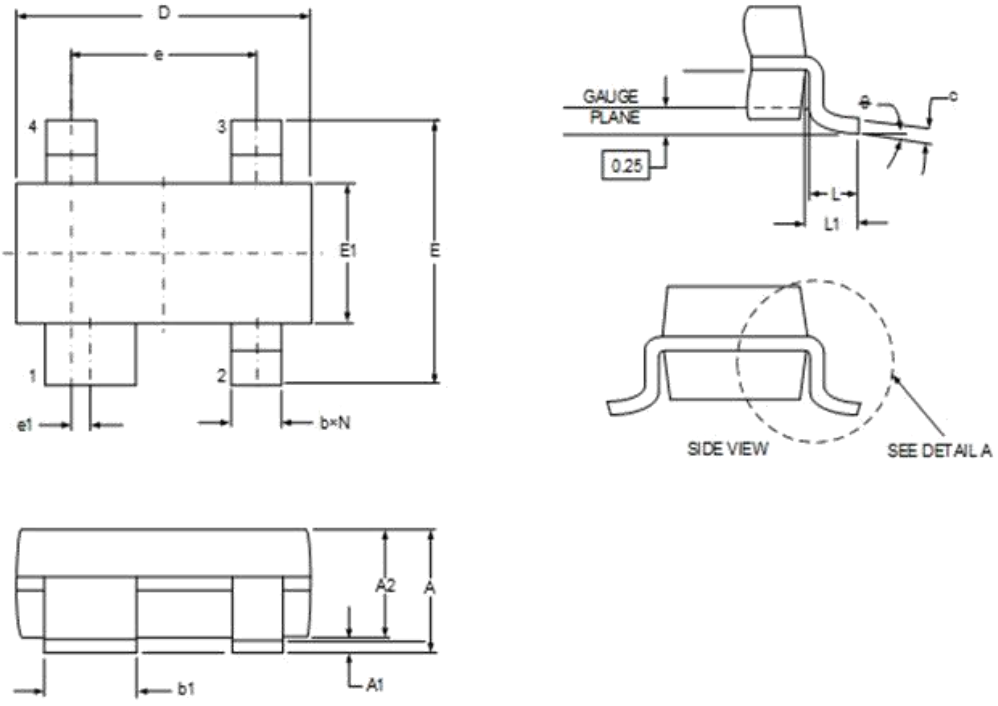
### RESET Valid at Low Voltage

A resistor can be added from the $\overline{\text{RESET}}$ pin to ground to ensure the $\overline{\text{RESET}}$ output remains low with VCC down to 0V. A 100kΩ resistor connected from the $\overline{\text{RESET}}$ to ground is recommended. The size of the resistor should be large enough not to load the output excessively and small enough to pull-down any stray leakage currents.



# Mechanical Dimensions

**SOT-143 Package Information**




| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MILLIMETER | | INCHES | |
| | MIN | MAX | MIN | MAX |
| A | 0.900 | 1.150 | 0.035 | 0.045 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.050 | 0.035 | 0.041 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| b1 | 0.750 | 0.900 | 0.030 | 0.035 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.800 | 3.000 | 0.110 | 0.118 |
| e | 1.800 | 2.000 | 0.071 | 0.079 |
| e1 | 0.200TYP | | 0.008TYP | |
| E | 2.250 | 2.550 | 0.089 | 0.100 |
| E1 | 1.200 | 1.400 | 0.047 | 0.055 |
| L1 | 0.550REF | | 0.022REF | |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| θ | 0° | 8° | 0° | 8° |