The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

U12

PART_NUMBER=CY7C68013A

USB CONTROLLER

U9

PART_NUMBER=XC2C256

PARALLEL TO SERIAL CONVERTER

USB CONNECTOR

USB TYPE B RECEPTACLE

NOTE: EMBEDDED VERSION IS NOT BUS POWERED

TARGET INTERFACE CONNNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
AND EMBEDDED_TMS WITH LVDS BUFFERS.

LEGEND:

- (01) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- ● COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- ● OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

NOTE:

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (01) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST.
J1 DOES NOT NEED TO BE PROGRAMMED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

Embedded USB JTAG: USB Controller, CPLD

Drawing Number: 0381242	
Date: 14-JUNE-2006	Ver: C
Sheet Size: D	Rev: 01
Sheet 14 of 16	Drawn By SCHWEIGLER

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