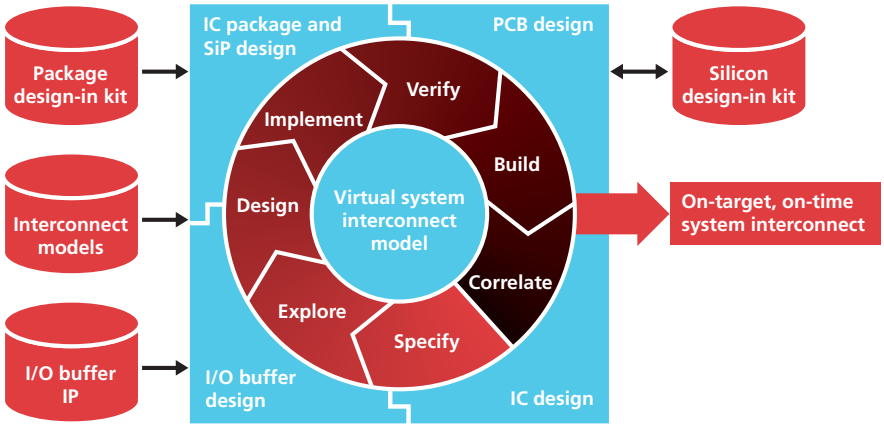
DATASHEET

ALLEGRO PCB DESIGN L, XL

Cadence® Allegro® PCB Design suites are complete, high-performance printed circuit board (PCB) design solutions. By employing the latest technology, they provide an interactive, constraint-driven environment for creating and editing complex, multilayer, high-speed, high-density PCBs. They allow users to define, manage, and validate critical high-speed signals at any stage of the design process and master today's most challenging PCB design issues. The results are increased productivity, shorter design cycles, and faster ramp up to volume production.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform's unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

PCB DESIGN SOLUTION

PCB designers face unprecedented challenges. Not only has design complexity intensified but also virtually all new designs contain high-speed signals that require careful management. Today's advanced designs also typically incorporate reusable intellectual property (IP) blocks and imported design modules for RF subcircuits. To deal with all this complexity, designers must be able to define and constrain critical high-speed signals at any stage of the design process, use sophisticated signal integrity (SI) and analysis tools, and ensure that the final PCB meets performance goals regarding traditional manufacturing and test specifications.

The Allegro PCB Design suites are complete design environments for implementing and solving these design challenges. Each provides a fully integrated design flow from design entry to a common electrical constraint management environment to auto/interactive PCB floorplanning to powerful auto/interactive routing. They are driven by electrical topology templates that define the optimum operating requirements of high-speed digital interconnect.

BENEFITS

- Proven, scalable, cost-effective PCB design solution
- Provides a complete interconnect environment for floorplanning and routing
- Speeds design with high-speed rules/constraints
- Includes a comprehensive feature set
- Features a front-to-back constraint management system

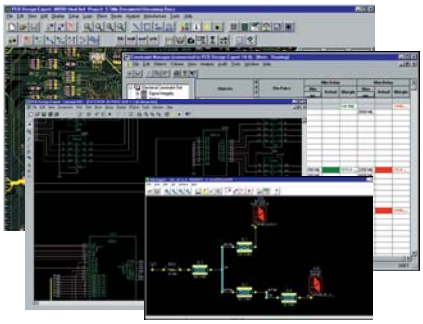
FEATURES

PCB EDITING

At the heart of Allegro PCB Design suites is Allegro PCB Editor, an interactive, high-speed, constraint-driven environment for creating and editing complex, multilayer PCBs. Its extensive feature set addresses a wide range of today's design and manufacturability challenges.

Allegro PCB Editor provides a powerful and flexible set of floorplanning tools. PCB design partitioning technology provides a concurrent design methodology for faster time to market and reduced layout time. Powerful shape-based shove/hug interactive etch creation/editing provides a highly productive interconnect environment while providing real-time, heads-up displays of length and timing margins.

Dynamic shape capability offers real-time copper pour plowing/healing functionality during placement and routing iterations. Allegro PCB Editor can generate a full suite of photo-tooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats.

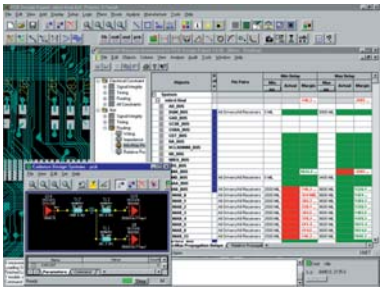


Allegro PCB Design suites bring together all the tools needed to design high-speed, constraint-driven PCBs

HIGH-SPEED CONSTRAINTS

Allegro Constraint Manager displays high-speed rules and their status (based on the current state of the design) in real time and is available at all stages of the design process. Each worksheet provides a spreadsheet interface that enables the user to capture, manage, and validate the different rules in a hierarchical fashion. This powerful application allows designers to graphically create, edit, and review constraint sets as graphical topologies that act as electronic blueprints of an ideal implementation strategy. Once the constraints are present in the database, they are used to drive the placement and routing processes for those signals.

Constraint Manager is completely integrated with the Allegro PCB Editor and high-speed rules can be checked in real time as the design process proceeds, with the results presented as part of the Constraint Manager spreadsheets. Any design parameters that do not meet their associated constraint values are highlighted. At any point during the design phase, users can launch the Constraint Manager to add, view, and manage high-speed constraint information associated with the design. Constraint Manager also displays the results of design analysis in real time alongside the constraint values in the spreadsheet, and color codes the results to indicate success or failure. This allows designers to immediately see the impact of any design changes in the spreadsheet.



Allegro Constraint Manager allows designers to manage high-speed constraints

ADVANCED FLOORPLANNING AND PLACEMENT

The Allegro PCB Editor's constraint and rules-driven methodology drives a powerful and flexible set of placement capabilities, including interactive and automatic component placement. The engineer or designer can assign components or subcircuits to specific rooms during design entry or floorplanning. Components can be filtered and selected by reference designator, device package/footprint style, associated net name, part number, or the schematic sheet/page number. With real-time design-for-assembly (DFA) analysis, Allegro PCB Editor offers real-time package-to-package clearance checking during interactive component placement. Driven from a two-dimensional spreadsheet array of classes and package instances, real-time feedback provides minimum clearance requirements based on the package's side-to-side, side-to-end, or end-to-end profiles.

With thousands of components on today's boards, real-time DFA analysis feedback increases the designer's productivity and efficiency by placing components to corporate or EMS guidelines. Allegro PCB Editor and Constraint Manager provide real-time graphical feedback of interconnect timing margins during interactive floorplanning. As a result, the PCB designer can simultaneously place devices for optimum routability, manufacturability, and signal timing.

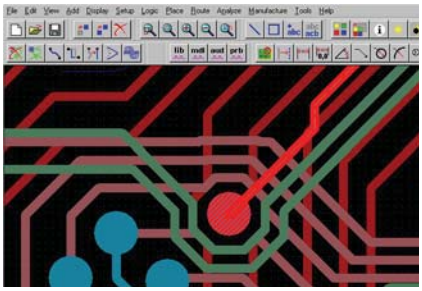
DESIGN PARTITIONING

The increasing deployment of globally dispersed design teams compounds the problems associated with shortening design cycle times. PCB design partitioning technology provides a concurrent design methodology for faster time to market and reduction in layout time. Using this technology, multiple designers working concurrently on a layout share access to a single database, regardless of team proximity. This can dramatically reduce overall design cycles and accelerate the design process.

Manual workarounds that address multiuser challenges are time consuming, slow and prone to error. Cadence Allegro PCB Design suites allow designers to partition designs into multiple sections or areas for layout and editing by several design team members. As a result, each designer can view all partitioned sections and update the design view for monitoring the status and progress of other users' sections.

INTERACTIVE ETCH EDITING

The interactive routing capability of Allegro PCB Editor provides powerful, interactive features that deliver controlled automation to maintain user control, while maximizing routing productivity. Real-time, shape-based, any angle, push/shove routing enables users to choose between "shove-preferred," "hug-preferred," or "hug-only" modes. Shove-preferred mode allows users to construct the optimum interconnect path while the real-time, shape-based router takes care of dynamically pushing obstacles. Routes will automatically jump over pins or vias. Hug-preferred mode is the perfect solution when a databus needs to be constructed. In hug-preferred mode, the router contour follows other interconnect as a priority and only pushes aside or jumps obstacles when there is no other option. The hug-only option performs like the hug-preferred mode, but without the push-and-shove aggression on other etch objects. The real-time, embedded, shape-based routing engine optimizes the route by either pushing obstacles or contour-following obstacles while dynamically jumping vias or component pins. Any interconnect that has high-speed constraints provides the designer with a real-time, graphical heads-up display that shows how much timing slack remains. Allegro PCB Editor's interactive routing also provides the ability to perform group routing on multiple nets and interactive tuning of nets with high-speed length or delay constraints.



Dynamic push-and-shove capabilities make interactive editing easy on even the most advanced designs

DYNAMIC SHAPES

Allegro PCB Editor's Dynamic Shape technology offers real-time copper pour plowing/healing functionality. Shape parameters can be applied at three different levels. Parameters are structured into global, shape instance, and object-level hierarchies. Traces, vias, and components added to a dynamic shape will automatically plow and void through the shape. When items are removed, the shape will automatically fill back in. Dynamic shapes do not require batch auto-voiding or other post-processing steps after edits are made.

PCB MANUFACTURING

Allegro PCB Editor can generate a full suite of photo-tooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats. More importantly, Allegro PCB Editor supports the industry initiative towards Gerber-less manufacturing through its Valor ODB++ interface that includes the Valor Universal Viewer. The ODB++ data format creates accurate and reliable manufacturing data for high-quality, Gerber-less manufacturing.

SYSTEM REQUIREMENTS

- Pentium 4 (32-bit) equivalent or faster
- Windows XP Professional, Windows XP Home Edition, or Windows 2000 (SP4)
- Minimum 256MB RAM (512MB recommended)
- 300MB swap space (or more)
- CD-ROM drive
- 32,768 color Windows display with minimum 1024 x 768 (1280 x 1024 recommended)

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

ALLEGRO PCB EDITOR FEATURE SUMMARY

	PCB Design Suite L Series	PCB Design Suite L Series Options	PCB Design Suite XL Series
Netlist/Crossplace/Cross-probe with Allegro Design Entry (HDL or CIS)	x		x
Padstack and Symbol Editor	x		x
Customizable/Automated Drill Legend	x		x
Multiple Via Sizes, Blind/Buried Via Support	x		x
Autoplacement/Quickplace/Floorplanner	x		x
Dynamic Shapes with Real-Time Plowing and Healing for Copper Areas	x		x
Automatic Line Smoothing	x		x
2-D Drafting and Dimensioning	x		x
Gerber 274X, 274D Artwork Output Generation	x		x
Multiple UNDO/REDO	x		x
Valor ODB++, ODB++(X) File Output & Universal Viewer	x		x
HTML-based Reports	x		x
Exposed Copper DRC	x		x
Interactive Etch Editing	x		x
Automatic Silkscreen Generation	x		x
Split Plane Support	x		x
SKILL Runtime, Macro, and Script Support	x		x
Variant Editor for Defining Different Variants of The Design (Allegro Design Entry HDL)	x		x
Assembly Drawing Creation for Each Variant	x		x
Bill-of-Materials Generation for Each Variant	x		x
Agilent EEsof Integration	x		x
CAD Interfaces - DXF (Ver. 14), IDF (Ver. 2 & 3), IFF	x		x
PCB Interfaces - PADS (Ver. 4 & 6), PowerPCB (Ver. 5), P-CAD (Ver. 8)	x		x
Length, Parallelism, and Differential Pairs Rule Support		PCB Performance	x
Pin-pair Multi/Matched Nested Group Support		PCB Performance	x
Real-time DRC and Routing of Differentail Pairs amd Length Rules		PCB Performance	x
Interactive Delay Tuning		PCB Performance	x
Complex Physical Design Rule Checking (No Electrical)		PCB Performance	x
Group Routing		PCB Performance	x
Measure Parasitic		PCB Performance	x
Advanced Trace Glossing		PCB Performance	x
Database-driven Design Reuse Modules		PCB Performance	x
Technology Files		PCB Performance	x
Design for Assembly Rule Checking		PCB Performance	x
TestPrep for Testability Access		PCB Performance	x
Allegro Constraint Manager (Routing Constraints and DRC Worksheets)		PCB Performance	x
Allegro PCB Router High-speed Routing Alignment (6U)		PCB Performance	x
Real-time DRC of Delay and Crosstalk Rules		PCB Performance	x
Constraint Areas and Technology File Support		PCB Performance	x
Automatic Line Width Adjustment for Impedance Rules		PCB Performance	x
eXtended Net Support (x-nets)		PCB Performance	x
Layer Set Rules and Routing Support		PCB Performance	x
Delay, Crosstalk, and Impedance Routing Support			x
Allegro Constraint Manager (Routing, SI, and Timing Constraints and DRC Worksheets)			x
Z-Axis Delay Support			x
Extended Timing Path Support			x
Group Routing (Space Control)			x
Differential Pair (Dynamic Phase Control)			x
Dynamic Design-for-Assembly Analysis (Real-time Feedback)			x
Display and Spread Segments Over Voids			x
Back Drilling Support			x
PCB Design Partitioning Technology	PCB Partitioning option*		PCB Partitioning option

Front-end Options Summary

	PCB Design Suite L Series	PCB Design Suite L Series Options	PCB Design Suite XL Series
Allegro Design Entry HDL OR Allegro Design Entry CIS	x		x
Allegro Constraint Manager (Allegro Design Entry HDL only)			x
Part Developer/Component Management	x		x
Allegro Design Entry HDL Rules Checker			x

** PCB Performance Option Required*

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or Cadence Channel Partner in your area, visit www.cadence.com/contact_us.

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